INTELTRONIC

3.5 inch TFT LCD
with Capacitive Touch Panel
SPECIFICATION

MODEL NAME: LMTD2035CHN1- GCD1

Date: 2012 / 08 / 09

Customer Signature		
Customer		
Approved Date	**Approved By**	**Reviewed By**

CTP Module Specification

Preliminary

ITEM NO.: LMTD2035CHN1-GCD1

Table of Contents

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment
1	9/AUG/12’			Initial Preliminary

3. GENERAL SPECIFICATIONS

Composition: 3.5 inch HVGA resolution display with a projected Capacitive Touch Panel (CTP).
Interface：The RGB Interface for display and I^2C for the CTP.

Parameter	Specifications	Unit
Screen Size	3.5 (diagonal)	inch
Display Format	320(H) x (R,G,B) x 480(V)	dot
Outline Dimension	100 (W)x 58 (H)x 4.1 (D)	mm
LCD Active Area	73.44 (W) ×48.96 (H)	mm
Sensor Active Area	76.43 (W) x 51.09 (H)	mm
Pixel Pitch	0.153(W) × 0.153(H) mm	mm
Type	Transparent type projected capacitive touch panel	
Input mode	Human's finger	
Pixel Configuration	Stripe	
Back-light	LED	
TFT-LCD Display mode	Normally white , Transmissive	
Weight	36	g
TFT-View Angle direction(Gray inversion)	12 o'clock	

4. LCD ABSOLUTE MAXIMUM RATINGS

GND=0V

Parameter	Symbol	MIN.	MAX.	Unit	Note
Power supply voltage	IOVCC	-0.3	4.6	V	
	VCC	-0.3	4.6	V	
Logic Input voltage	VIN	-0.3	IOVCC+0.3	V	
Backlight Forward Current	IF		25	mA	For each LED
Operating temperature	Topr	-20	70	℃	
Storage temperature	Tstg	-30	80	℃	

5. LCD ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
I/O pin Power Supply Voltage	IOVCC	I/O pin Operation Voltage	1.65	2.8	3.3	V
Analog Power Supply Voltage	VCC	Analog Operation Voltage	2.5	2.8	3.3	V
Logic High level input voltage	VIH	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3*IOVCC	V
Logic High level Output voltage	VOH	Iout = -1 mA	0.8*IOVCC	-	IOVCC	V
Logic Low level Output voltage	VOL	Iout = -1 mA	0.0	-	0.2*IOVCC	V

5.2 Current Consumption

Ta= 25°C

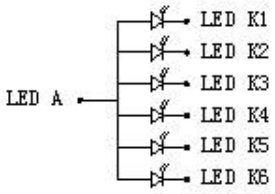
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Current for Power Supply Voltage	I_{IOVCC}	--	--	5	mA	
	I_{VCC}	--	--	10	mA	

5.3 Backlight Driving Consumption

Ta= 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_F		3.2		V	
LED current	I_F	-	20	-	mA	For each LED
LED dice Life Time		30000			hr	Note2

Note 1:



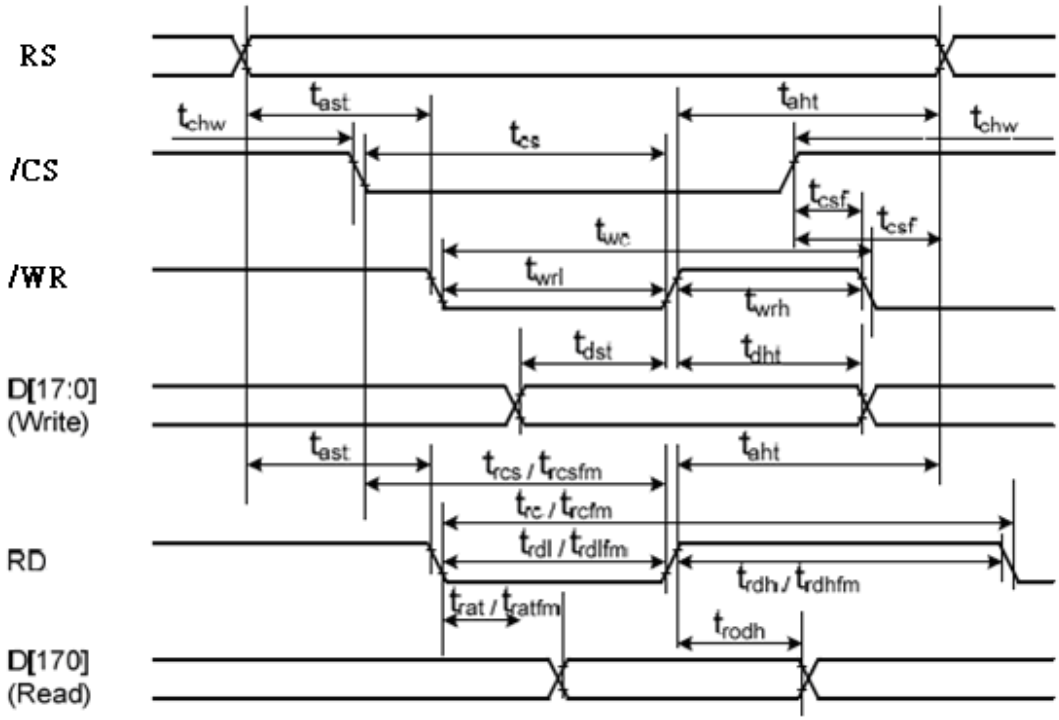
Note 2:

The “LED dice life time” is defined as the brightness decrease to 50% original brightness that the ambient temperature is 25℃ and LED dice current=20mA.

6. LCD TIMING SPECIFICATIONS

6.1 AC Characteristics

6.1.1 DBI Type B Interface Timing Characteristics

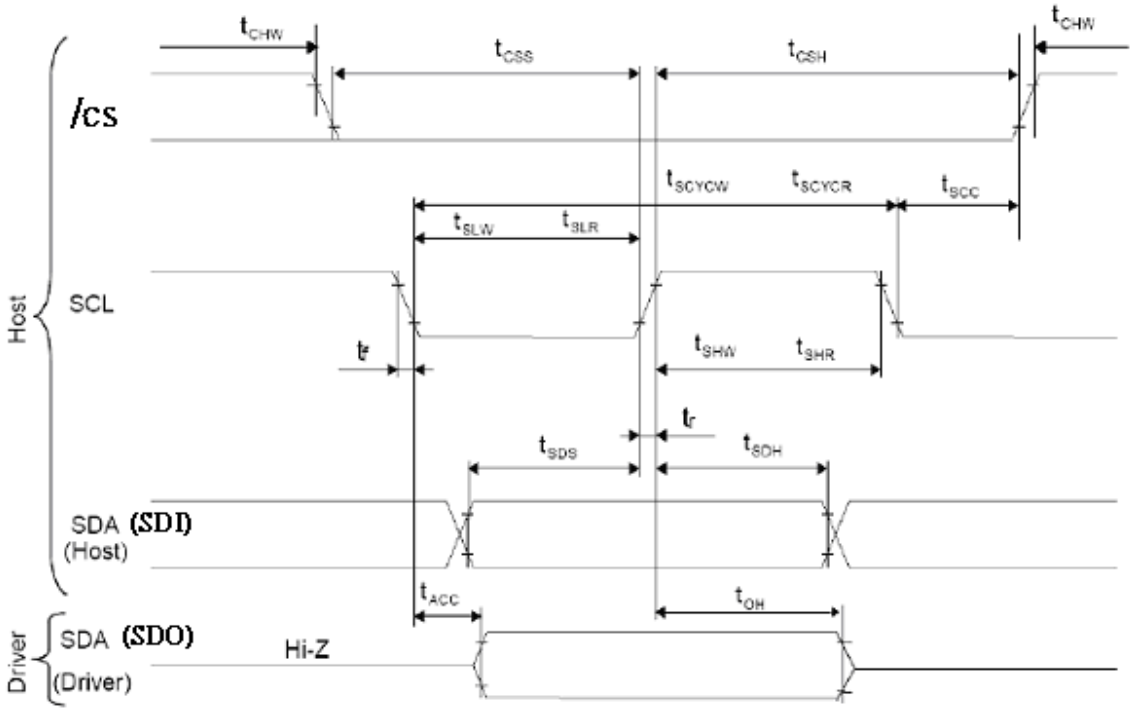


Signal	Symbo l	Parameter	min	max	Unit	Description
RS	tast	Address setup time	10	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
/CS	tchw	/CS pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	Trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	
/WR	twc	Write cycle	50	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RD(FM)	Trcfm	Read cycle	450	-	ns	When read from frame memory
	Trdhfm	Read Control pulse H duration	90	-	ns	
	Trdlfm	Read Control pulse L duration	355	-	ns	
RD(ID)	Trc	Read cycle	160	-	ns	When read ID data
	Trdh	Read Control pulse H duration	90	-	ns	
	Trdl	Read Control pulse L duration	45	-	ns	
DB[17:0],	Tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	Tdht	Write data hold time	10	-	ns	
	Trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCC=2.5V to 3.3V, GND=0V
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

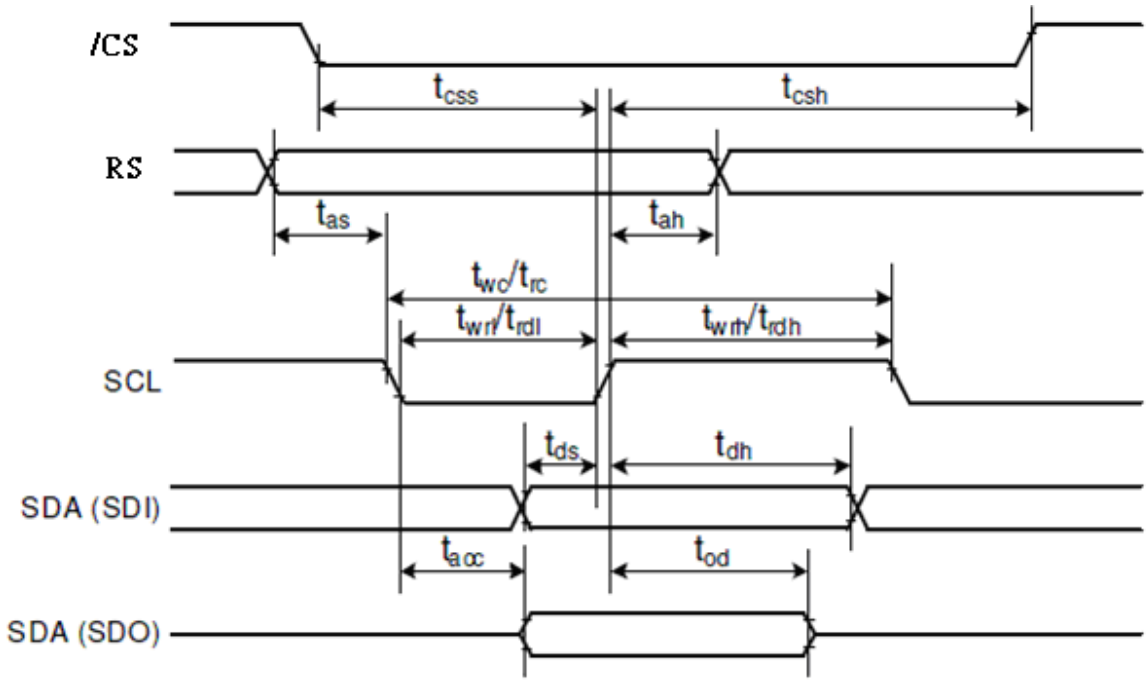
6.1.2 DBI Type C Interface Timing Characteristics

6.1.2.1 3-Line SPI



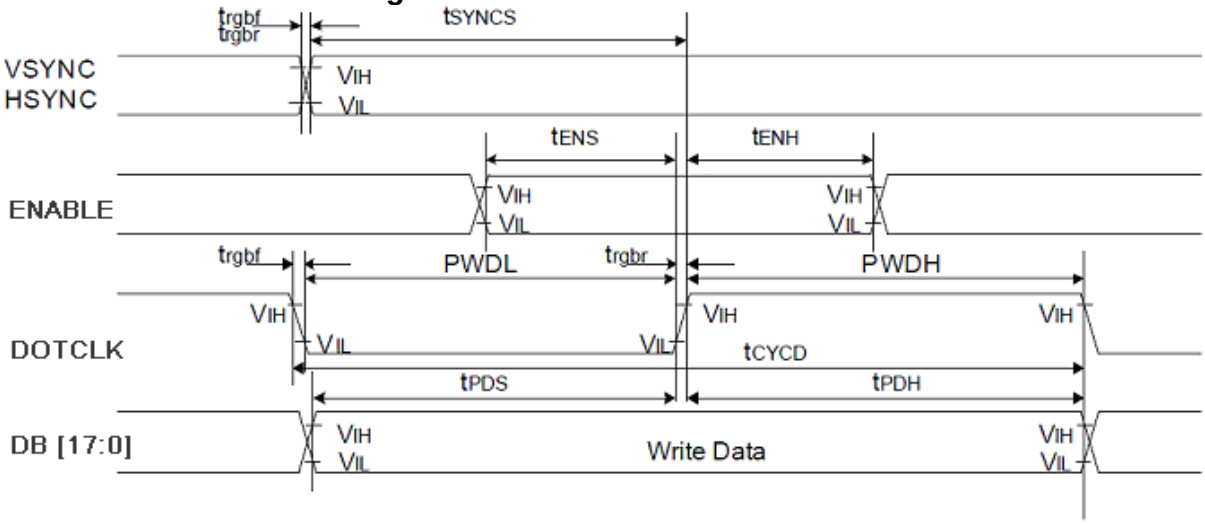
Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	66		ns	
	tshw	SCL “H” Pulse Width (Write)	15		ns	
	tslw	SCL “L” Pulse Width (Write)	15		ns	
	tscycr	Serial Clock Cycle (Read)	150		ns	
	tshr	SCL “H” Pulse Width (Read)	60		ns	
	tslr	SCL “L” Pulse Width (Read)	60		ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10		ns	
	tsdh	Data hold time (Write)	10		ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	
	toh	Output disable time (Read)	15	50	ns	
/CS	tscc	SCL- /CS	15		ns	
	tchw	/CS “H”Pulse Width	40		ns	
	tcss	/CS -SCL Time	60		ns	
	tcsh		65		ns	

6.1.2.1 4-Line SPI



Signal	Symbol	Parameter	min	max	Unit	Description
/CS	tcss	Chip select time (Write)	15		ns	
	tcsh	Chip select hold time (Read)	60		ns	
SCL	twc	Serial Clock Cycle (Write)	66		ns	
	twrh	SCL “H” Pulse Width (Write)	15		ns	
	twrl	SCL “L” Pulse Width (Write)	15		ns	
	trc	Serial Clock Cycle (Read)	150		ns	
	trdh	SCL “H” Pulse Width (Read)	60		ns	
	trdl	SCL “L” Pulse Width (Read)	60		ns	
RS	tas	RS setup time	10		ns	
	tah	RS hold time (Write / Read)	10		ns	
SDA / SDI (Input)	tds	Data setup time (Write)	10		ns	
	tdh	Data hold time (Write)	10		ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

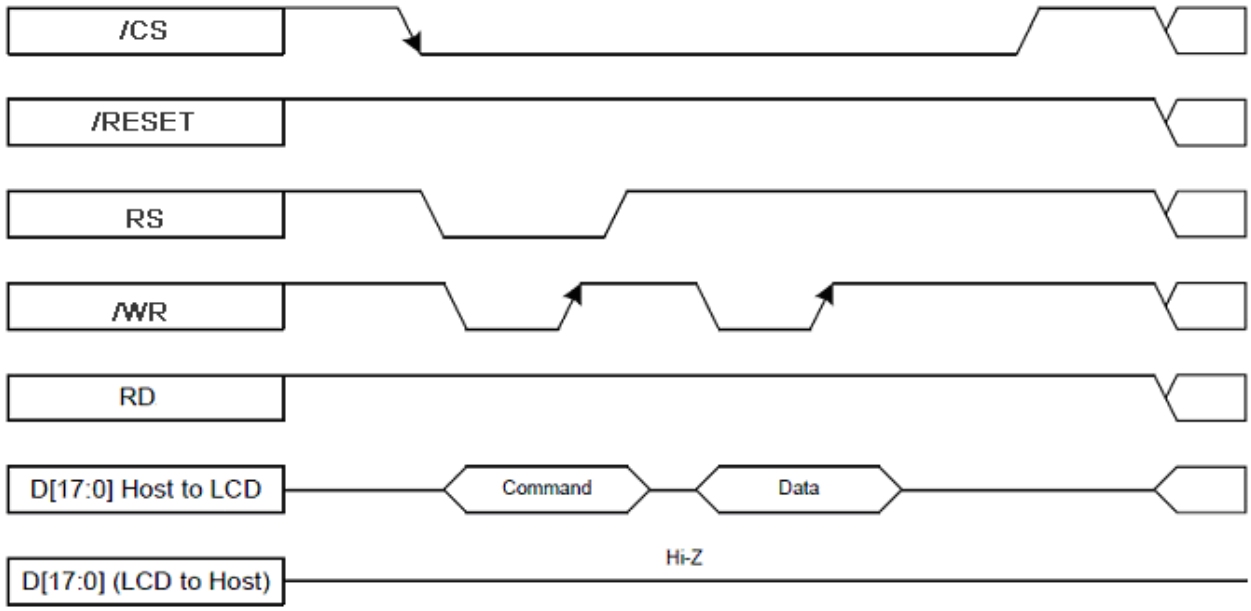
6.1.3 DPI Interface Timing Characteristics



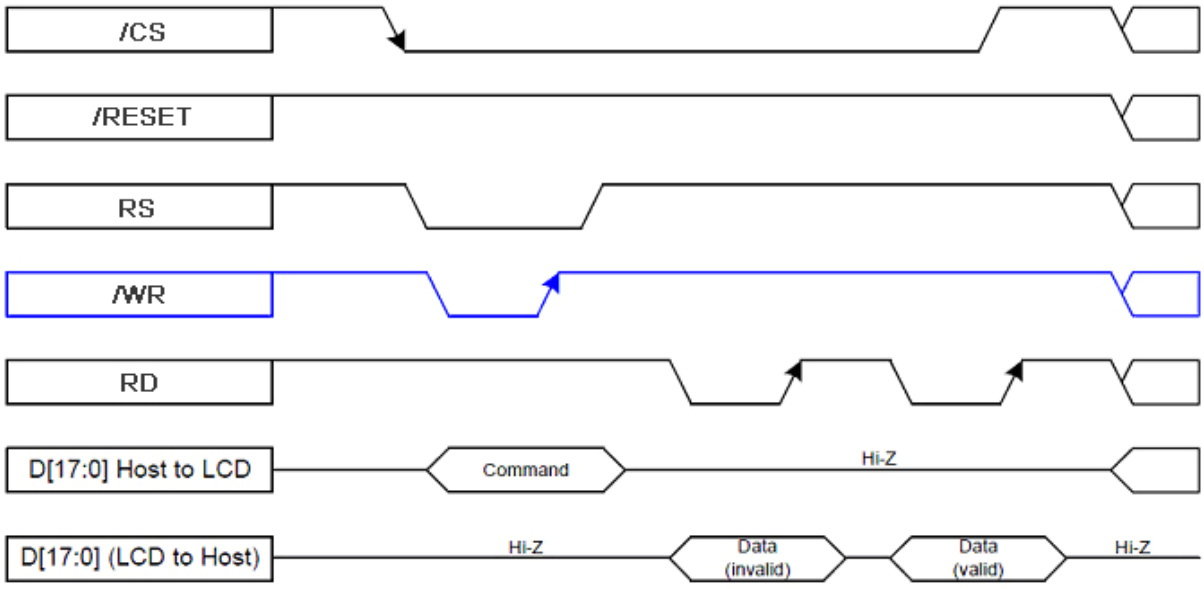
Signal	Symbol	Parameter	min	max	Unit
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns
	t_{ENH}	ENABLE hold time	15	-	ns
DB[17:0]	t_{POS}	Data setup time	15	-	ns
	t_{PDH}	Data hold time	15	-	ns
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns
	PWDL	DOTCLK low-level period	15	-	ns
	t_{CYCD}	DOTCLK cycle time	66	-	ns
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns

6.2 Display Bus Interface (DBI)

6.2.1 Write Cycle



6.2.2 Read Cycle



Note: Read Data is only valid when the RS input is pulled high. If RS is driven low during read then the display information outputs will be High-Z.

6.2.3 DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

			First Transfer									Second Transfer								
	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

8-bit data bus DB[7:0] interface, IM[2:0] = 011

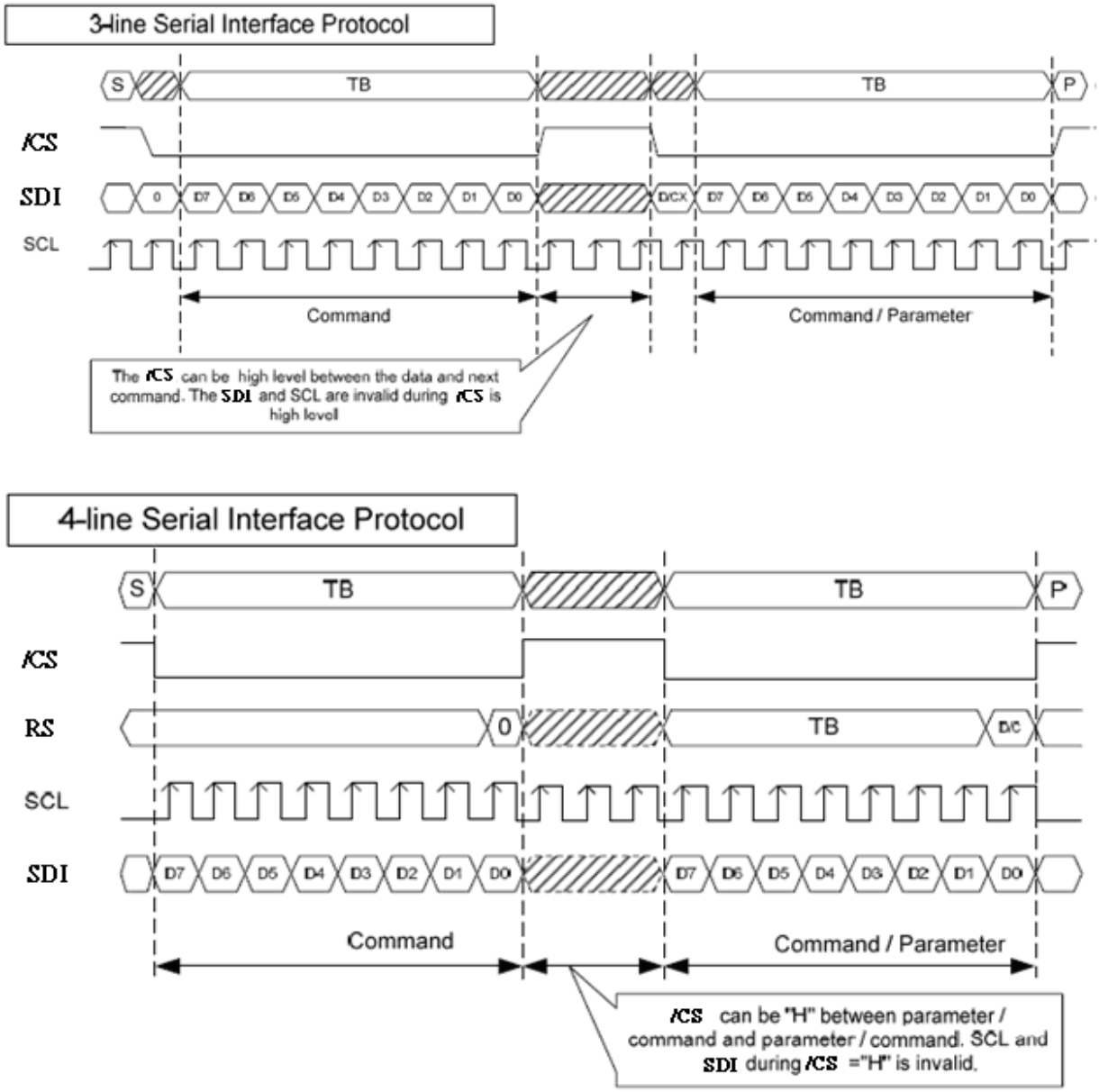
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

			First Transfer								Second Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

			First Transfer								Second Transfer								Third Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

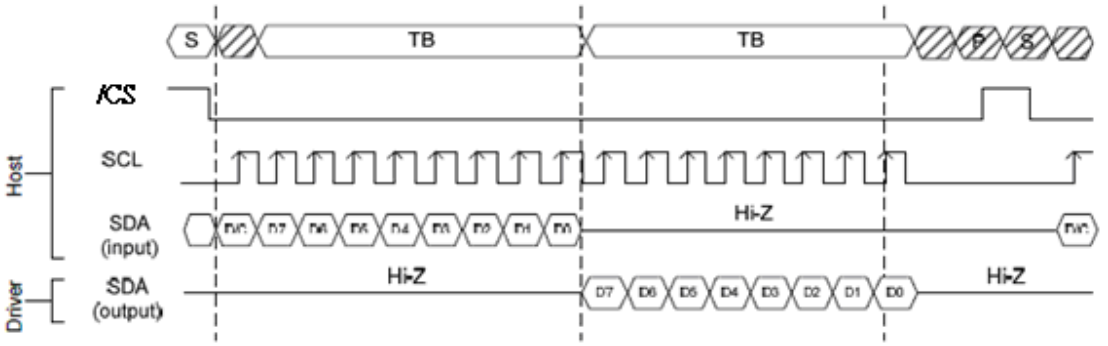
6.3 Serial Interface (Type C)

6.3.1 Write Cycle and Sequence

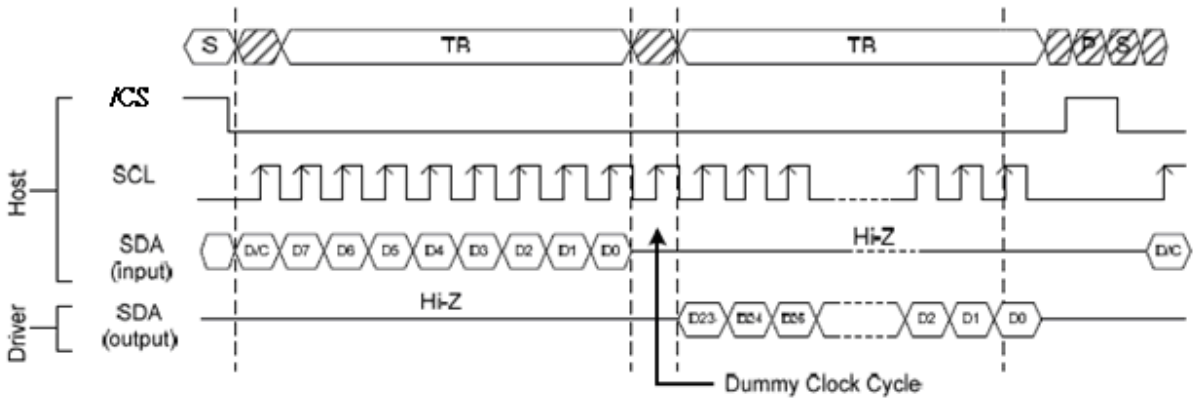


6.3.2 Read Cycle and Sequence

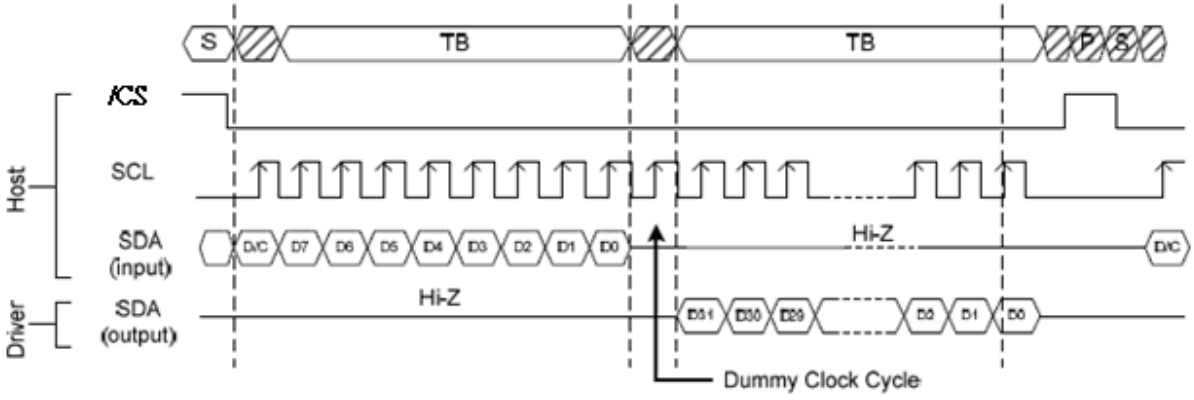
3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



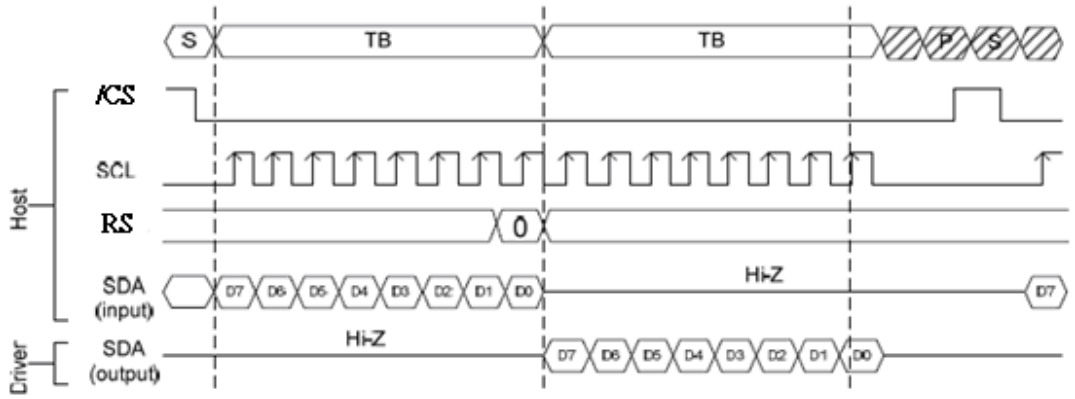
3-line Serial Protocol (for RDDID command: 24-bit read)



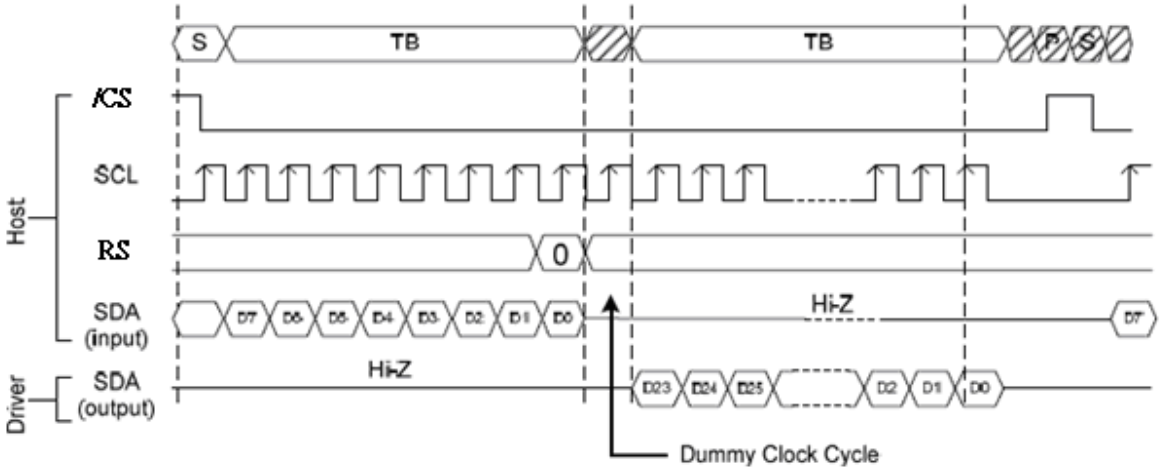
3-line Serial Protocol (for RDDST command: 32-bit read)



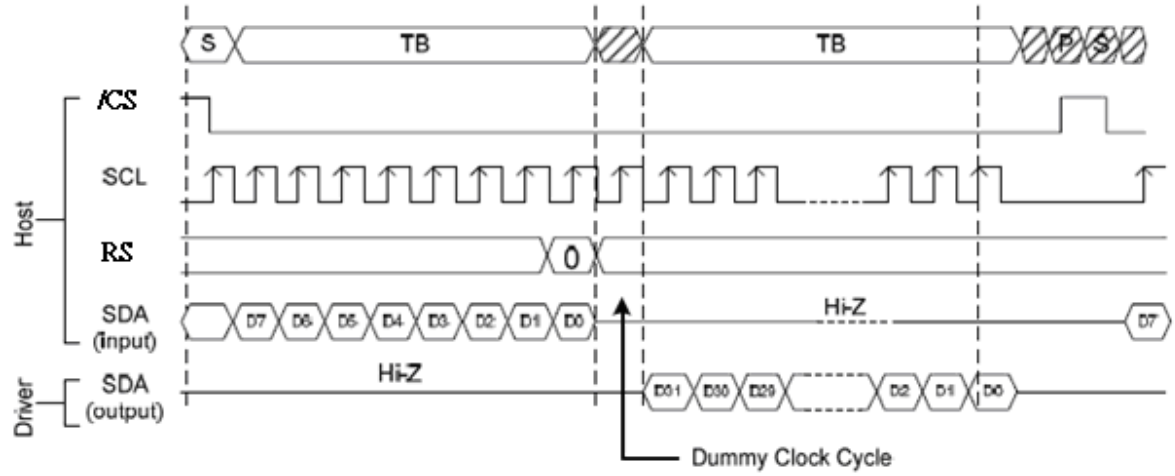
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



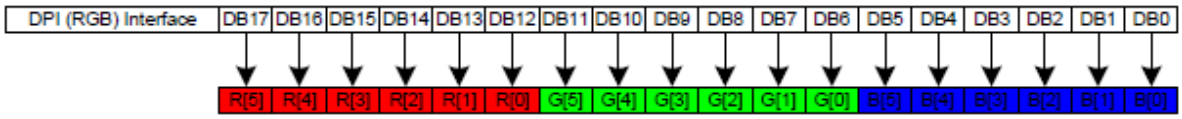
4-line Serial Protocol (for RDDID command: 24-bit read)

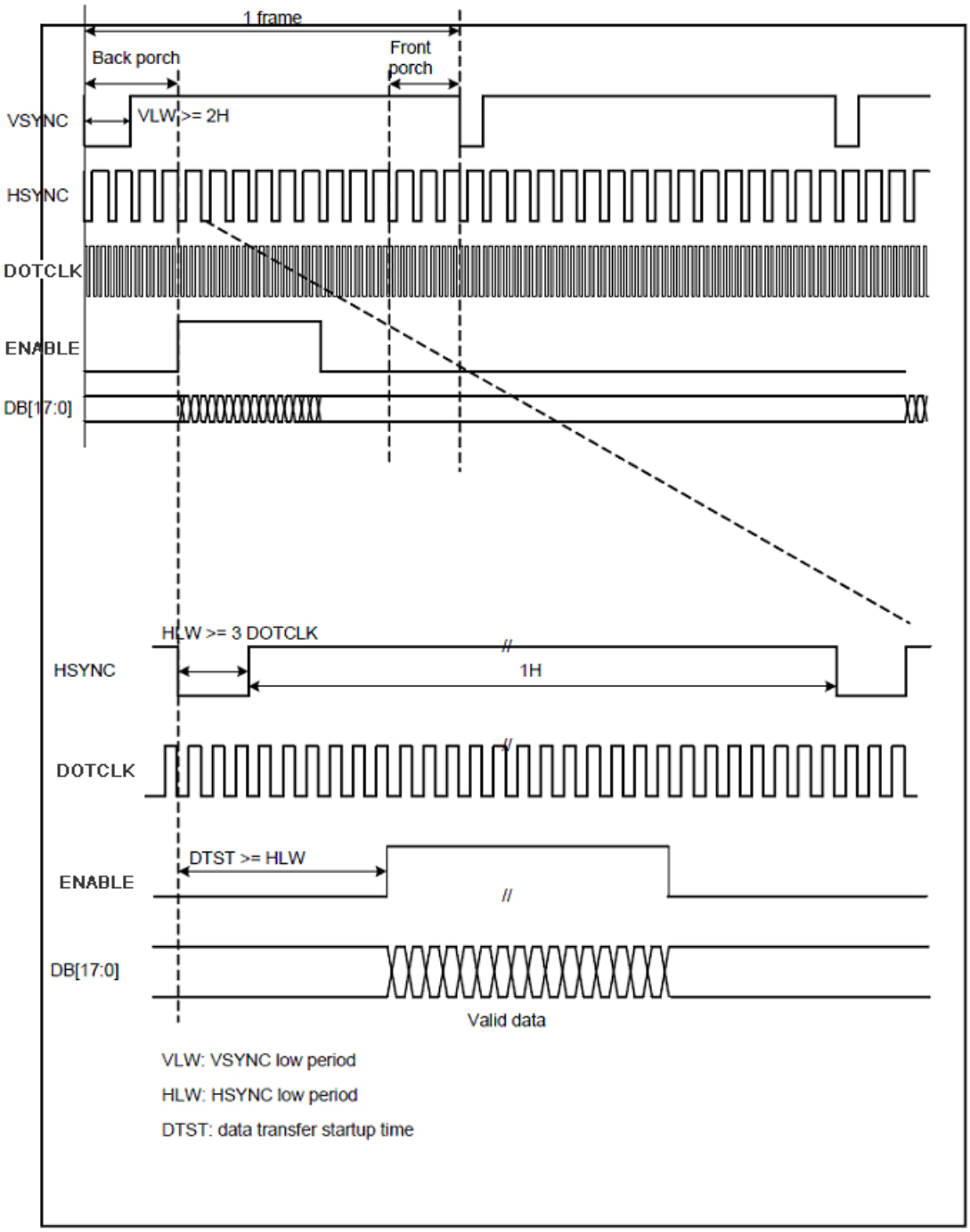


4-line Serial Protocol (for RDDST command: 32-bit read)



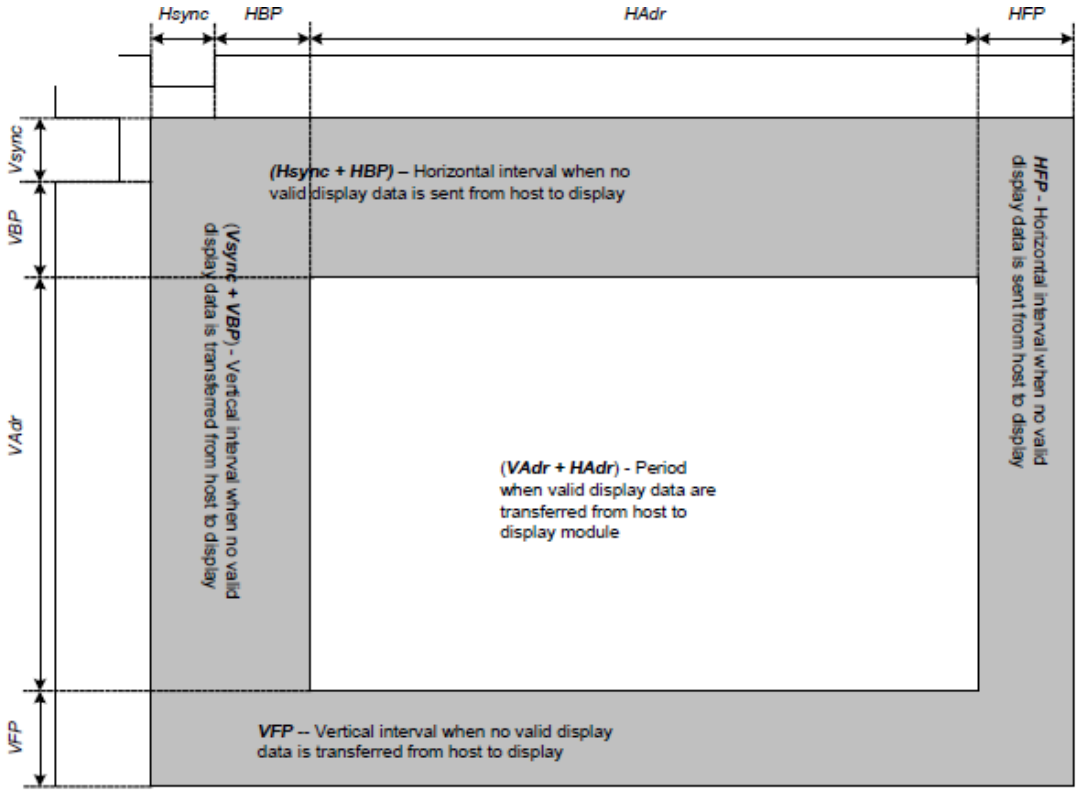
6.4 Display Pixel Interface (DPI)





Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

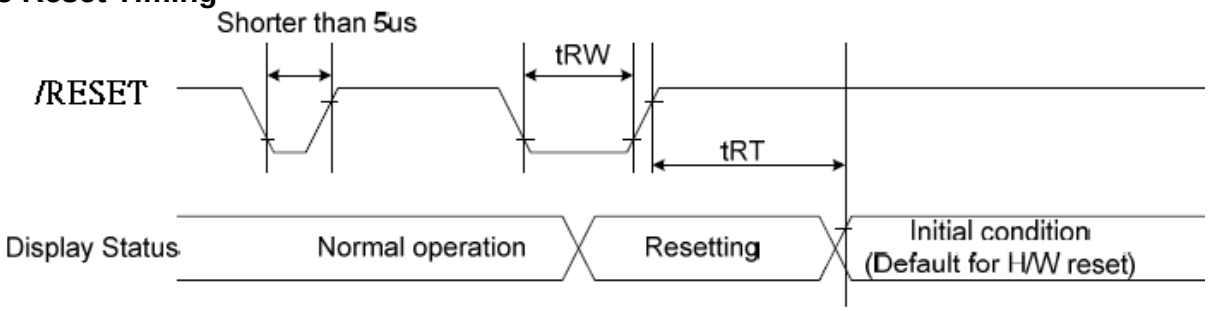
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.



ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
DOTCLK frequency		10	12.5	15	MHz
DOTCLK cycle	DOTCLK CYC	66.6	80	100	ns
HSYNC pulse width	Hsync	2	2	-	PCLK
HSYNC Back Porch	HBP	3	3	-	PCLK
Horizontal Display Area	Hadr	320	320	320	PCLK
HSYNC Front Porch	HFP	3	3	-	PCLK
Horizontal Frequency		-	33		KHz
VSYNC pulse width	Vsync	2	2	-	Line
VSYNC Back Porch	VBP	2	2		Line
Vertical Display Area	Vadr	480	480	480	Line
VSYNC Front Porch	VFP	2	2	-	Line
Vertical Frequency		50	60	80	Hz

Notes:
1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals DOTCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

6.5 Reset Timing



Signal	Symbol	Parameter	Min	Max.	Unit	Note
/RESET	tRW	Reset pulse duration	10		us	
	tRT	Reset cancel		5	ms	1, 5
				120	ms	1, 6, 7

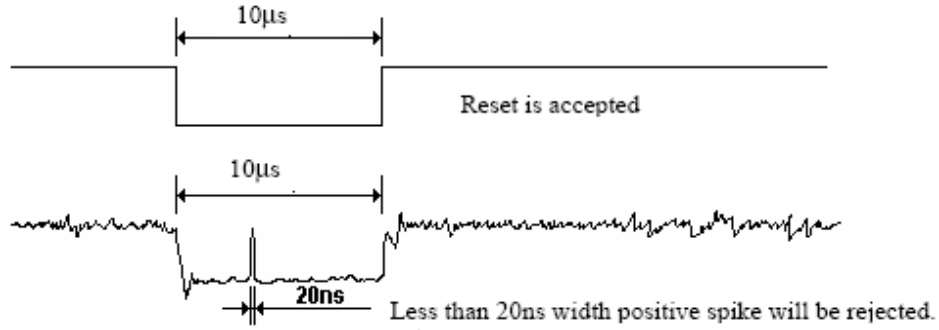
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of /RESET.

Note 2: Spike due to an electrostatic discharge on /RESET line does not cause irregular system reset according to the table below:

/RESET Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.
Note 6: When Reset applied during Sleep Out Mode.
Note 7: It is necessary to wait 5msec after releasing /RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD PIN CONNECTIONS

7.1 PIN CONNECTIONS TABLE

Pin No	Symbol	I/O	Description	Remark
1	FLM	O	Output a frame head pulse signal. If no used, please open this pin	
2	GND	P	Ground	
3	ENABLE	I	Data enable signal in RGB mode If no used, please fix this pin at GND level	
4	DOTCLK	I	Pixel clock signal in RGB mode If no used, please connect this pin to GND	
5	VSYNC	I	Vertical sync. signal in RGB mode If no used, please connect this pin to GND	
6	GND	P	Ground	
7	HSYNC	I	Horizontal sync, signal in RGB mode If no used, please connect this pin to GND	
8	IM0	I	Interface mode select	Note2
9	IM1	I		
10	IM2	I		
11	IOVCC	P	IO POWER	
12	VCC	P	Analog POWER	
13	SDI	I/O	Serial data in/out pin in DBI Type C 9bit mode Serial data input pin in DBI Type B 8bit mode If no used, please connect this pin to GND	
14	SDO	O	Serial data output pin If no used, please connect this pin to GND	
15	DB17	I/O	Data Bus	
16	DB16	I/O		
17	DB15	I/O		
18	DB14	I/O		
19	DB13	I/O		
20	DB12	I/O		
21	DB11	I/O		
22	DB10	I/O		
23	DB9	I/O		
24	DB8	I/O		
25	DB7	I/O		
26	DB6	I/O		
27	DB5	I/O		
28	DB4	I/O		
29	DB3	I/O		
30	DB2	I/O		
31	DB1	I/O		
32	DB0	I/O		
33	/RESET	I	Reset pin	
34	RD	I	Read strobe signal If no used, please connect this pin to IOVCC	
35	/WR/SCL	I	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVCC	
36	RS	I	Data/command selection pin	
37	/CS	I	Chip select signal	
38	LEDK6	P	LED CATHODE	
39	LEDK5	P		

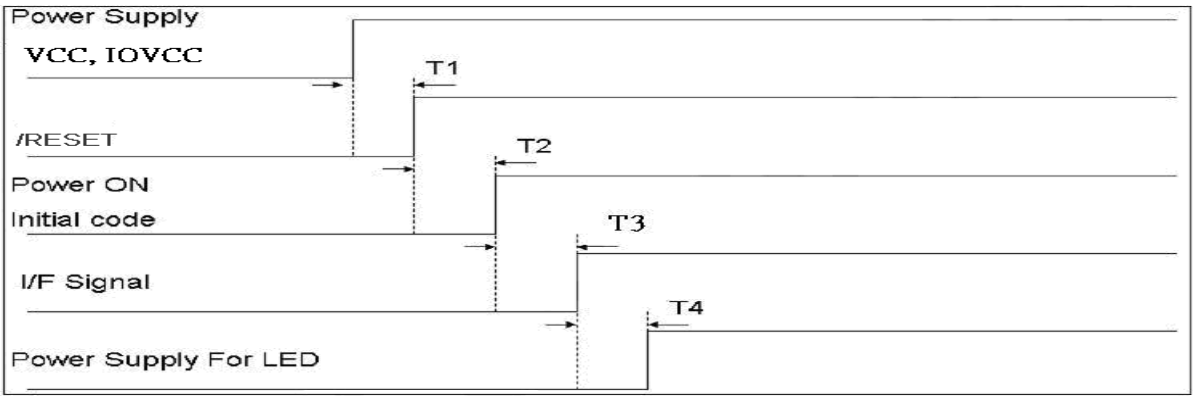
40	LEDK4	P		
41	LEDK3	P		
42	LEDK2	P		
43	LEDK1	P		
44	LEDA	P	LED ANODE	
45	LCM_ID	O	Ground	

I/O definition：I-----Input; O---Output; P----Power
Note1：No used I/O pin please fix to GND level
Note2：

IM2	IM1	IM0	Interface Mode	DB Pin in use
0	0	0	DBI Type B 18-bit	DB [17:0]
0	0	1	DBI Type B 9-bit	DB [8:0]
0	1	0	DBI Type B 16-bit	DB [15:0]
0	1	1	DBI Type B 8-bit	DB [7:0]
1	0	1	DBI Type C 3-line SPI	SDI, SDO
1	1	1	DBI Type C 4-line SPI	SDI, SDO

7.2 power ON/OFF sequence:

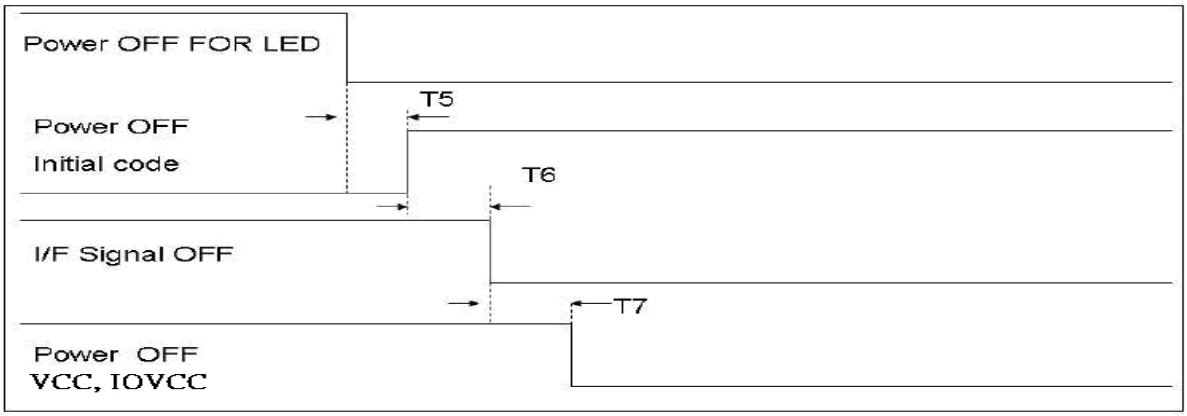
Power on:



10ms≦T1≦20ms ; 50ms≦T2≦100ms

100ms≦T3≦200ms ; 100ms≦T4≦200ms

Power off:



50ms≦T5≦100ms; 50ms≦T6≦100ms
100ms≦T7≦200ms

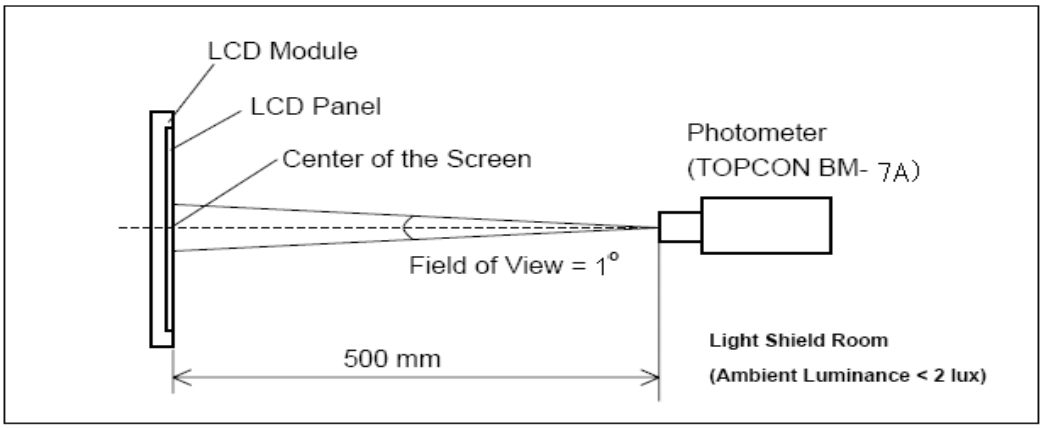
8. OPTICAL CHARACTERISTIC

Ta=25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Contrast Ratio		CR	Viewing normal angle θx=θy =0°	400	500		-	Note2
Response Time		T_R		-	5		ms	Note3
		T_F		-	15		ms	
Viewing Angle	Hor.	θx+	Center CR≥10	-	70	-	deg	Note4
		θx-		-	70	-		
	Ver.	θy+		-	60	-		
		θy-		-	60	-		
Brightness		L	θx=θy =0°	210	250	-	cd/㎡	Note5
Uniformity		B-uni	θx=θy =0°	70	80		%	Note6
Chromaticity	R	X_R	Center θx=θy =0°	0.591	0.641	0.691	-	
		Y_R		0.270	0.320	0.370	-	
	G	X_G	Center θx=θy =0°	0.250	0.300	0.350	-	
		Y_G		0.516	0.566	0.616	-	
	B	X_B	Center θx=θy =0°	0.084	0.134	0.184	-	
		Y_B		0.078	0.128	0.178	-	
	W	X_W	Center θx=θy =0°	0.247	0.297	0.347	-	
		Y_W		0.281	0.331	0.381	-	

Note 1: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 2-3 minutes in a windless room.

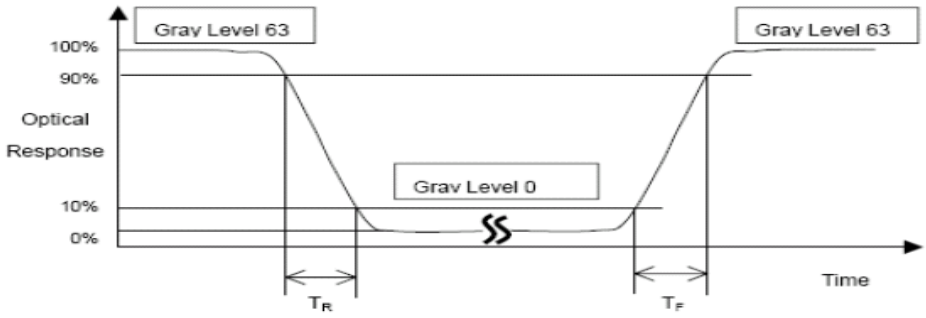


Note 2: Definition of contrast ratio:

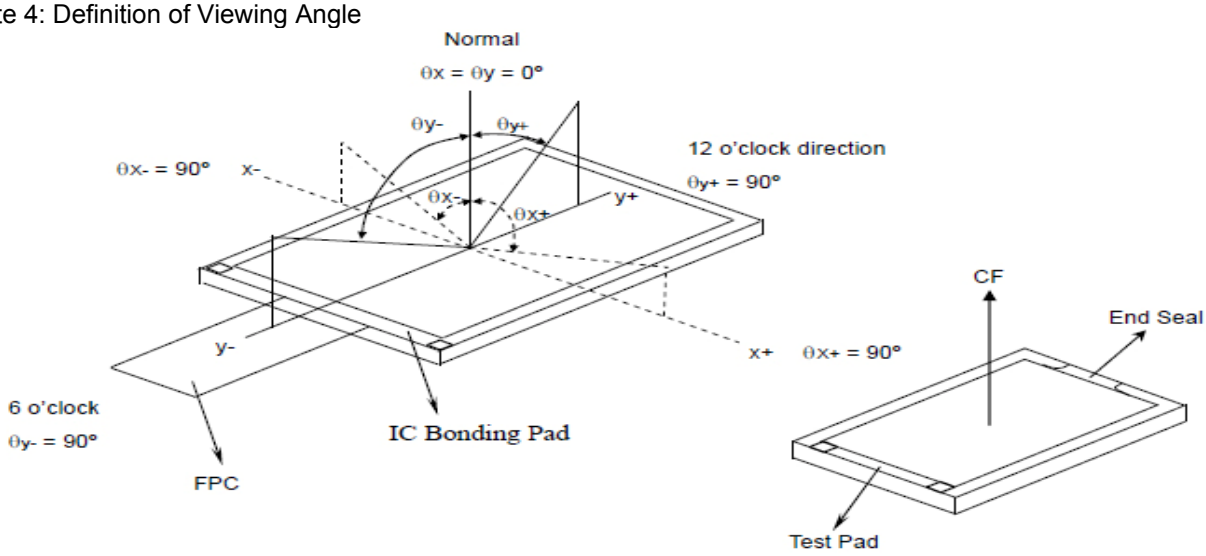
The contrast ratio is defined as following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Note 3: Definition of Response Time (TR,TF):

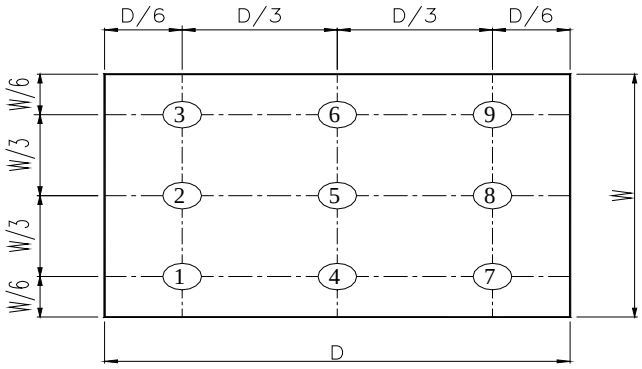


Note 4: Definition of Viewing Angle



Note 5: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

Note 6: Definition of Brightness Uniformity (B-uni)



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}}$$

9. CTP SPECIFICATIONS

9.1ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Typ	Max	Unit
VCC	Supply voltage	-0.3	-	3.6	V
VI	Logic input voltage	-0.3	-	Vcc+0.3	V

9.2ELECTRICAL CHARACTERISTICS

Symbol	Description	Min	Typ	Max	Unit
VCC	Supply voltage	2.5	3.3	3.6	V
GND	Supply voltage	-	0	-	V
VIH	Input H voltage	0.8Vcc	-	Vcc	V
VIL	Input L voltage	0	-	0.2Vcc	V
Icc	Vcc current	-	5	6	mA

9.3 I²C PROTOCOL SPECIFICATIONS

1. Supports 100 KHz clock frequency and up to 400 kHz (Fast Mode).
2. Only support single master solution.
3. Only support 7 bit addressing.
4. If I²C master can't finish 1byte data in 100ms, I²C slave will restart. The CTP controller operates only as a slave device. The I²C interface is functional in active and sleep modes. In sleep mode, asynchronous address match detector hardware allows a sleeping controller to recognize its address and wake up. And the firmware can implements different I²C touch protocols. The timings for example that as table 9.3.1
5. I²C slave can hold off the master in the middle of a transaction using what's called clock stretching (the slave keeps SCL pulled low until it's ready to continue). Refer to figure 9.3.2 for an example.
6. Slave device address = **0x5C**.

Table 9.3.1: I²C timing

Symbol	Parameter	Min	Typ	Max	Unit
TLOW	I²C clock low time	2 • TCPU			
THIGH	I²C clock high time	2 • TCPU			
THD,STA	I²C clock hold time	2 • TCPU			
TSU,STA	I²C start setup time				
TSU,STO	I²C stop setup time				
THD,DAT	I²C data hold time, when driven by master side				
TSU,DAT	I²C data setup time, when driven by master side				
TBUF	I²C bus free time	4.7			us
TCSR	I²C clock stretching release time	9 • TCPU			
TVD,DAT	I²C data valid after clock change, when data is driven by slave side	9 • TCPU			
TTCPU	CPU master clock period			55	ns

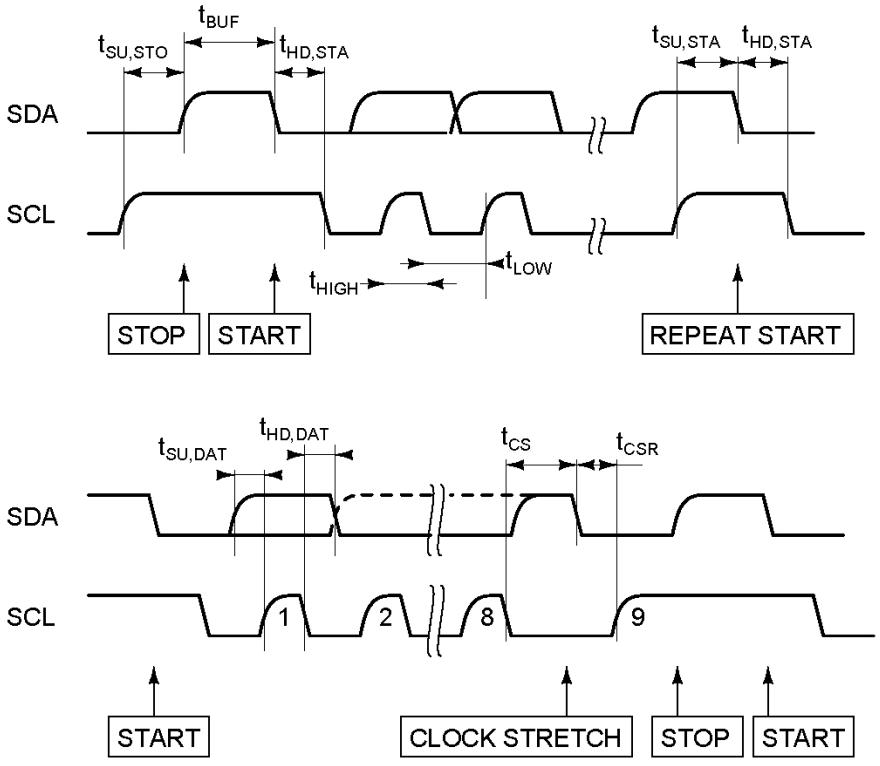


Figure 9.3.1: I²C clock stretching example

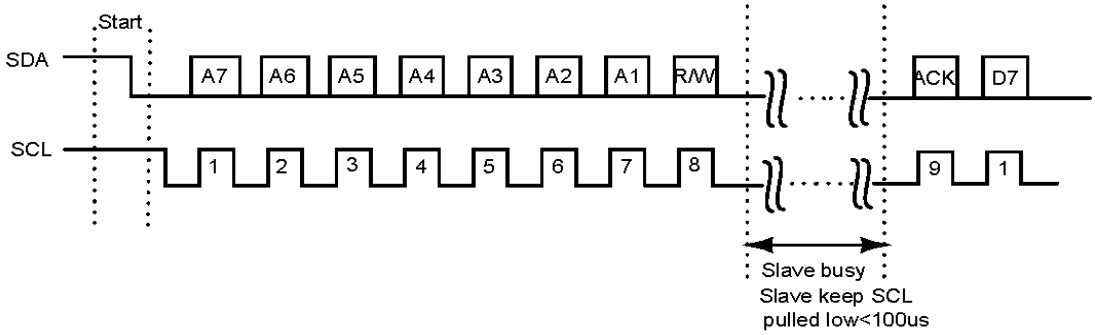


Figure 9.3.2: I²C clock stretching example

9.3.1. Data Protocol

The communication follows I²C convention. Refer to figure 9.3.3 for a definition of the symbols used.

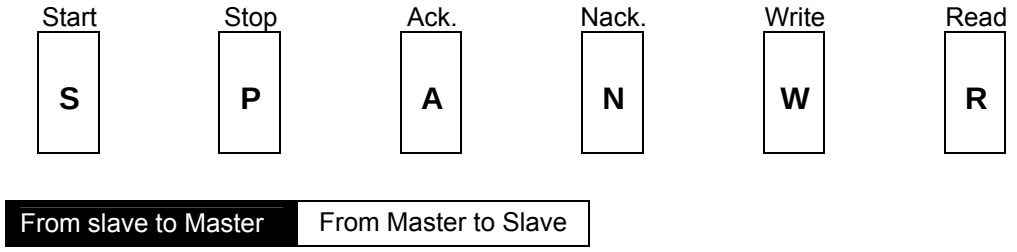


Figure 9.3.3: I²C symbols

9.3.2 Introduction

The protocol for data exchange has been designed with the following considerations

- Most of the data traffic is read operation to get the finger or fingers position.
- Read operation do need an initial write operation.
- Write operations are most of the time power management and interrupt setting instructions.
- Interrupt pulse width setting adjustments need a write operation.

9.3.2.1 Read operation

Read packets have variable content length, decided by the host. It is available to do a single read operation or a sequential read operation. Therefore, the beginning register address is needed to set before a read operation. And the data sent exactly follow the register table 9.4.2, table 9.4.5. And, the firmware in the slave will use a memory copy of the register for I²C slave read operation, so that firmware can continue updates, and I²C slave is still using a consistent (but old) coordinates for read operation.

- In a sequential read operation, the first data sent by the controller is therefore the touching register, and then the X and Y coordinates of the first finger, then 2nd finger, 3rd finger, 4th finger and then coordinates of the 5th finger, and so on. Referred in figure 9.3.5 .
- If the host do not finish the read operation when the INT line is set again, the slave firmware will delay to update coordinates registers for I²C read operation until the host finish the read operation. referred to first part of figure 9.3.6.
- I²C stop condition will release data protection and allow the slave firmware update the coordinates registers for I²C read operation. So, the host has the chance to get incorrect data when it get the coordinates data with single read operation. Because the host send many times of I²C stop condition in each multi-fingers coordinates position reading, it will give the slave firmware chance to update the coordinates registers for I²C read operation, the host will give a combines unrelated data (combines new and old coordinates together), referred to the second part of figure 9.3.6.

Figure 9.3.4: Read operation

Figure 9.3.5: Coordinates read operation

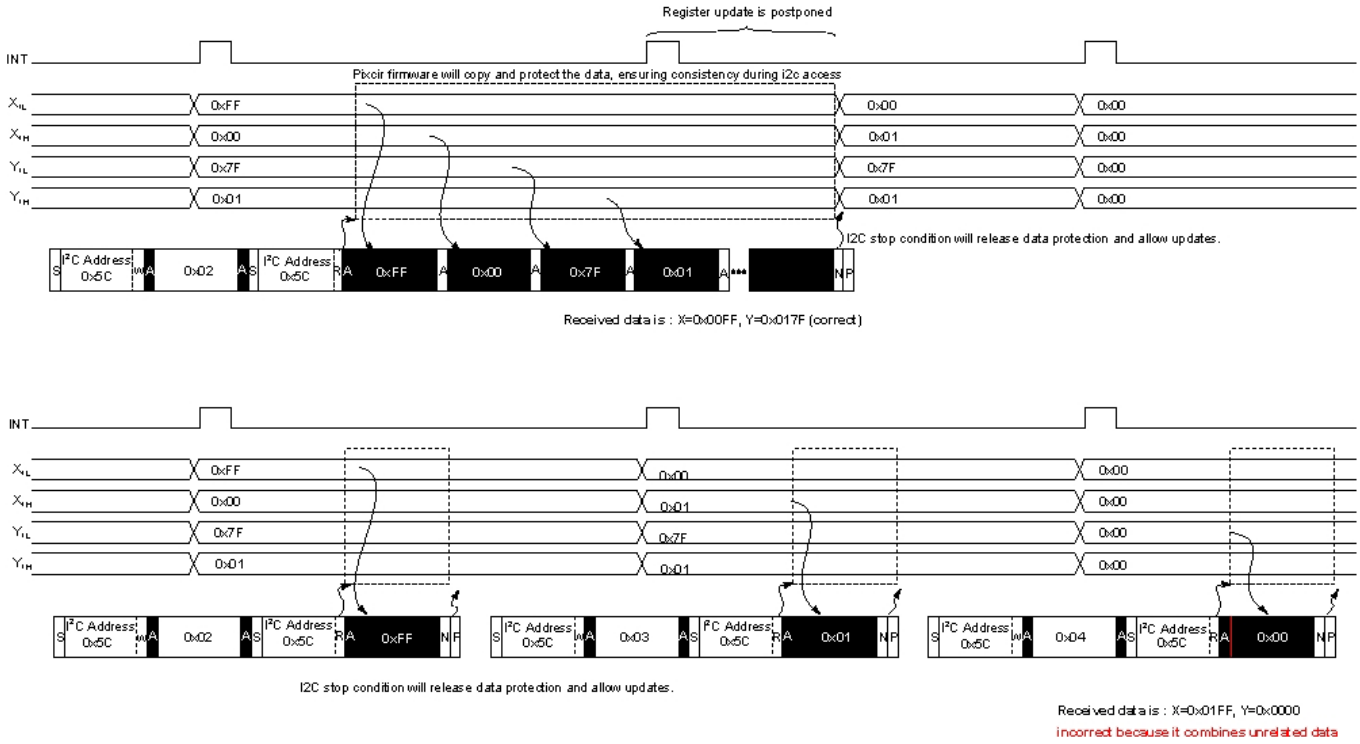


Figure 9.3.6: Coordinates read operation explanation

9.3.2.2 Write operation

Write packets have variable content length, decided by the host. Write operation stops when host issues an I²C STOP symbol. The write packet is illustrated in figure 9.3.7 and figure 9.3.8. Following the I²C device address, the first byte of the write packet is always the destination register address, referred in table 9.3.2, table 9.3.5. Subsequent data value are written at the register pointed by the address, immediately upon reception of the byte. The address counter is automatically incremented. Subsequent data bytes are treated in continuation of the writing operation.

Figure 9.3.7: Write operation.

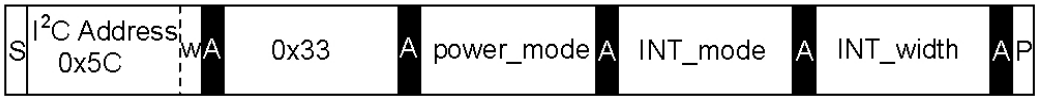


Figure 9.3.8: Write mode setting operation.

9.4 Registers

9.4.1 Endianness

Data are little endian, which means LSB byte appears before MSB byte.

9.4.2 Registers organization

The accessible registers are shown in the table 9.4.2, table 9.4.5. These registers are technically accessible both for reading or writing direction. However, most registers have only one meaningful direction: finger position registers, for example, are typically used in read direction, and writing to them will have no effect; their content will be overridden after a new sensor scan.

Table 9.4.2: registers table

Address	Type	Name	Description	Category
0	Char	Touching	Bit field, see table 9.4.3	Touch
1	Char	Buttons	Reserved	
2 (LSB) 3 (MSB)	Int	PosX1	Finger #1 X position	
4 (LSB) 5 (MSB)	Int	PosY1	Finger #1 Y position	
6	Char	ID1	Finger #1 identificator	
7 (LSB) 8 (MSB)	Int	PosX2	Finger #2 X position	
9 (LSB) 10 (MSB)	Int	PosY2	Finger #2 Y position	
11	Char	ID2	Finger #2 identificator	
27	Char	Strength1	Finger #1 strength	
28	Char	Strength2	Finger #2 strength	
32 (LSB) 33 (MSB)	Int	Initial_ distance	Distance separating fingers on the first time multi touch is detected	Gesture
34 (LSB) 35 (MSB)	Int	Distance	Distance separating fingers	
36 (LSB) 37 (MSB)	Int	Ratio	100˙distance / initial_ distance	
38	Char	Water_ level		Monitor
39	Char	Noise_ level		
40	Char	Palm_ level		
41	Char	Signal_ x		
42	Char	Signal_ y		
43 50	Char	Button1button8	Reserved	Buttons
51	Char	Power_ mode	Power management register. See table 9.4.6	power management
52	Char	INT_ mode	Control of the INT pin, see table 9.4.7	
53	Char	INT_ width	INT pulse width	
54	Char	Sleep_ freq	Scanning frequency in Sleep mode	
55	Char	Auto_ sleep_ delay	The delay time, the start is the last touch released in Active mode and the end is switch into Sleep mode successful	
56-57	Char		Reserved	Special operations
58	Char	SPECOP	Reserved	
59 (LSB) 60 (MSB)	Int	EEPROM_ read_ addr	Reserved	
61	Char	Engineering_ cmd	Allows, with I^2C, to send "hyper terminal like commands" for engineering modes	
62 (LSB) 63 (MSB)	Int	CRC	Reserved	version
64-68	Char	Version[0..31]	F/W Version Registers address 64 to 68 = (0x44, 0x38, 0x30, 0x30, 0x01)	
96-135	Char	Message[0..39]	Null terminated ASCII message string for engineering and debug purpose	

136 (LSB) 137 (MSB)	Int	RAW_CTRL	Controls RAW data mode (internal, raw, etc. . .) see table 9.4.4	
138	Char	Cross_ X	X coordinate for method 1 crossing node measurement request	Method 1
139	Char	Cross_ Y	Y coordinate for method 1 crossing node measurement request	
140 (LSB) 141 (MSB)	Int	Cross_ node	Measurement result for method 1	
142 (LSB) 143 (MSB)	Int	RAW[0..69] Shared with History_ buffer	Raw data, content controlled by RAW_CTRL register, or alternatively, history buffer (see Below)	RAW data
144 (LSB) 145 (MSB)	Int			
Etc.	Int			

Table 9.4.3: touching register (R0)

Bit 0,1,2	Nb of fingers touching (NBF)
Bit 3	Noise flag (indicates the report is unreliable) (NOI)
Bit 4	Message flag (indicates a message string is sent by slave) (MSG)
Bit 5	Buffer indicates the master has missed more than 2 reports, which are stored in buffer array (BUF)
Bit 6	Palm flag (indicates the algorithm has a palm or similar blocking issue) (PAL)
Bit 7	Water flag, indicates the algorithm has a rejected inputs due to water (WAT)

9.4.3 RAW_CTRL write & read

It is advised to use INT mode=0x08 when debug information are consulted (RAW_CTRL register not zero). Also, the slave can not instantly refresh the RAW tables following a modification by the master to the RAW_CTRL register, since in some conditions a relatively lengthy collection of measurements has to be performed. The master however can have the guaranty that the data reported in the RAW table reflects the request placed in RAW_CTRL if 2 INT pulses have elapsed. If the request in RAW_CTRL is unchanged, to every new INT pulse corresponds a refresh of the RAW table.

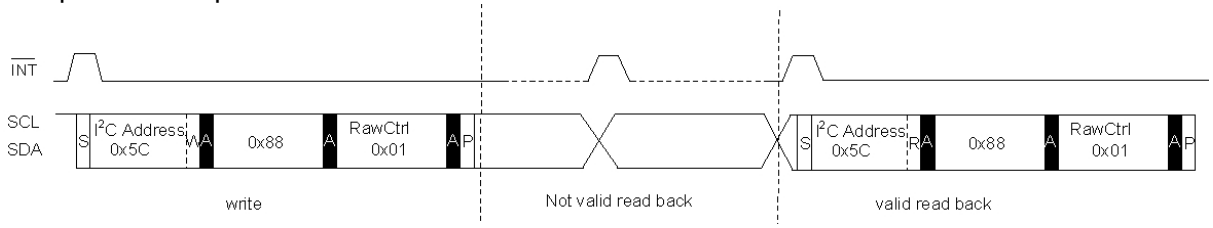


Figure 9.4.1: RAW_CTRL write & read

Table 9.4.4: RAW_CTRL (R136, 137)

Bit 0	Choose function (0: history buffer, 1: RAW data, 2: system info) See table 12.5
Bit 1	
Bit 2	Method (0 or 1)
Bit 3	Show offset correction (and low-pass filtering for M0)
Bit 4	Show m0 sensitivity adjustment (bit3 must also be set)
Bit 5	M1 pattern small (0) or pattern large (1)
Bit 6	M1 sense direction (0:Y,1:X)
Bit 7	M1 band scan. if 0, only report a single cross node. If 1,report a full X axis scan at RAW position
Bit 8	Disable Algorithm
Bit 9	Enable single shot RAW refresh, must be set to 1 and bit9 to 0. Auto back to 0 and bit9 to 1 after single shot is done
Bit 10	Refresh frozen after single shot is done when 1. Set to 0 to release the freeze and go back to normal refreshing
Bit 11	
Bit 12	
Bit 13	
Bit 14	
Bit 15	

Table 9.4.5: History buffer registers

Address	Type	Name	Description	Category
142	Char	Interval	Sub sampling rate when filling the history buffer. Disable: 0. Keep all points. 1. Keep one out of two. 2. Etc.	History buffer
143	Char	Buffer_ level	Number of fingers report in the buffer	
144 (LSB) 145 (MSB)	Int	Pos X	Coordinate X of the reported point, at time=0	
146 (LSB) 147 (MSB)	Int	Pos Y	Coordinate Y of the reported point, at time=0	
148 (LSB)	Int	Pos X	Coordinate X of the reported point at	

149 (MSB)			time=1	
150 (LSB) 151 (MSB)	Int	Pos Y	Coordinate Y of the reported point at time=1	
⋮	⋮	⋮	⋮	
298 (LSB) 299 (MSB)	Int	Pos X	Coordinate X of the reported point, at time=19	
300 (LSB) 301 (MSB)	Int	Pos Y	Coordinate Y of the reported point, at time=19	

9.4.4 Power_ mode register

The POWER_MODE register controls the power management and operation of the controller. However, modification becomes effective at any time. There are shown in the table 9.4.6

Table 9.4.6: Power_ mode register (R51)

Bit	Name	Description
7-3	-	Not used
2	ALLOW_SLEEP	Allow self demotion from active to sleep mode, provide that this flag is set. If the controller is in active mode and no finger is detected for more than IDLE_PERIOD time, then it allow automatically jumps to sleep mode. If this flag is not set, the host must explicitly switch the device from active to sleep mode.
1-0	POWER_MODE[1-0]	Power mode setting: 00: Active Mode 01: Sleep Mode 11: Freeze Mode

9.4.5 INT_ mode register

The slave can set the INT line, and host can read and write controller device, so the controller behaves like an I^2C slave device and fully complies with I^2C addressing and usual I^2C hand shake protocol. As such, controller is suitable in a bus shared with other I^2C slaves.

Table 9.4.7: INT_ mode register (R52)

Bit	Name	Description
7-4	-	Not used
3	EN_INT	0:disable interrupt mode 1:enable interrupt mode
2	INT_POL	0:the interrupt is low active(default) 1:the interrupt is high-active
1-0	INT_MODE[1-0]	00:INT assert periodically 01:INT assert only when finger moving(default) 10:INT assert only when finger touch 11: INT pulse assert only when finger touch

When INT_MODE=00 in the INT mode register, the slave will set the INT line with INT_ width pulse width after each scan in order to request the attention from the host, as shown in figure 9.4.1 and figure 9.4.2

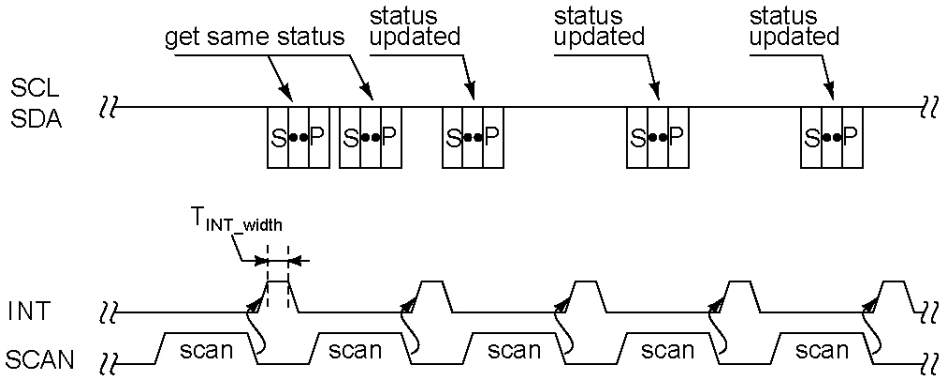


Figure 9.4.1: INT line pull up by slave (INT_POL=1,INT_MODE=00 in the INT mode register)

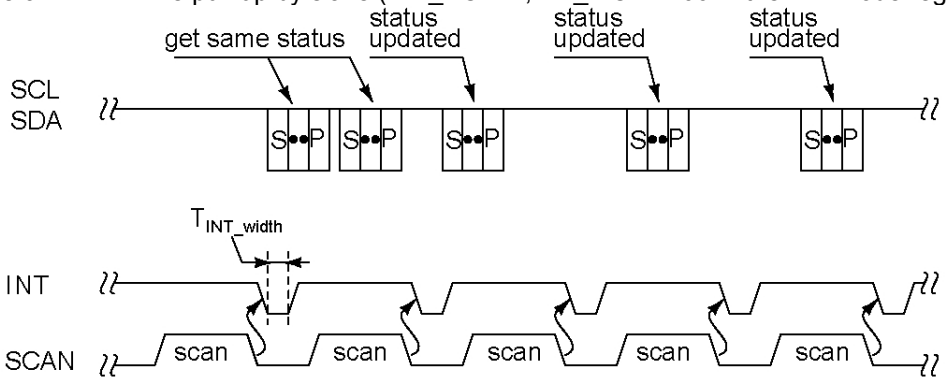


Figure 9.4.2: INT line pull down by slave (INT_POL=0, INT_MODE=00 in the INT mode register)

When INT_Mode=01 in the INT mode register and finger moving on the panel, the slave will set the INT line after each scan, as shown in figure 9.4.3 When finger leaves the panel, the slave will continue to pulse INT line for each scan; but once the master has serviced this request and become now aware that there is no more finger touching, the slave will stop pulse the INT line, and will also gradually reduce the scan speed, as shown in figure 9.4.4

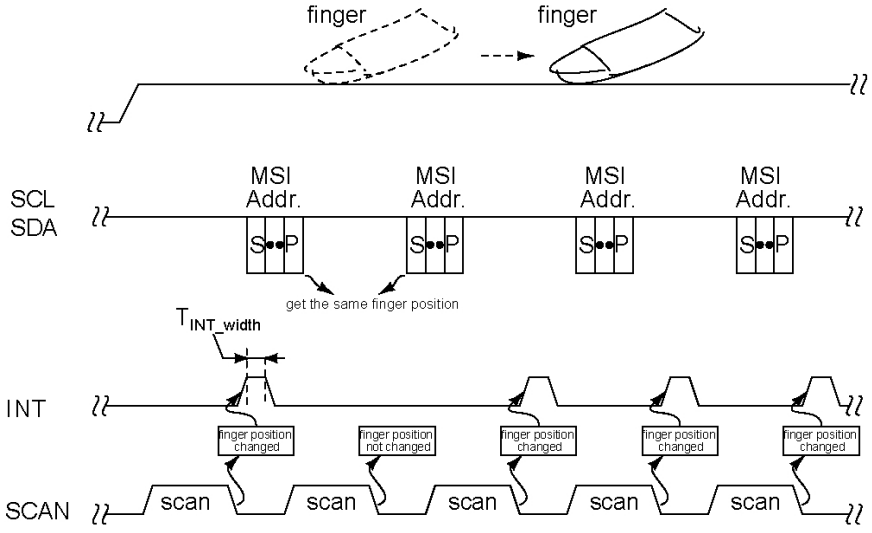


Figure 9.4.3: INT line pull up when finger moving (INT_POL=1, INT_MODE=01 in the INT mode register)

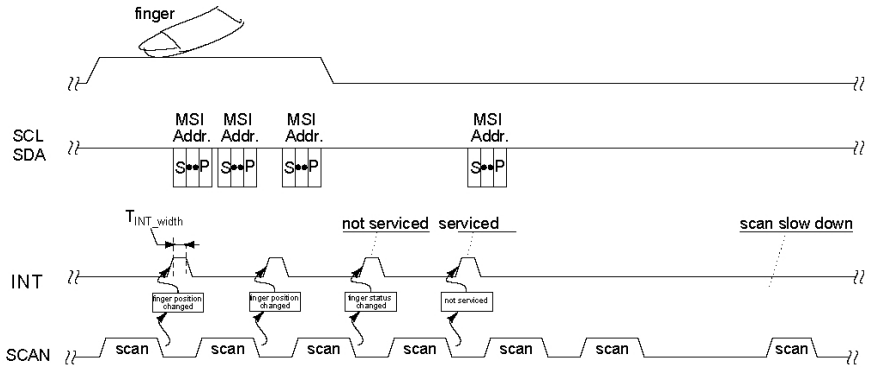


Figure 9.4.4: INT line will stop pulse when finger leaves and master has acknowledged the situation (INT_POL=1 in the INT mode register)

When INT_Mode=10 in the INT mode register and finger touch the panel, the slave will set the INT line after each scan, as shown in figure 9.4.5 When finger leaves the panel, the slave will continue keep INT line status for each scan; but once the master has serviced this request and become now aware that there is no more finger touching, the slave will release the INT line, and will also gradually reduce the scan speed, as shown in figure 9.4.6.

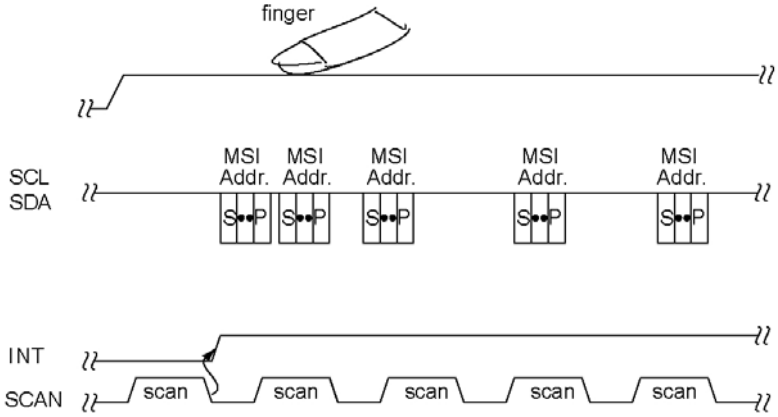


Figure 9.4.5: INT line pull up when finger touch (INT_POL=1, INT_MODE=10 in the INT mode register)

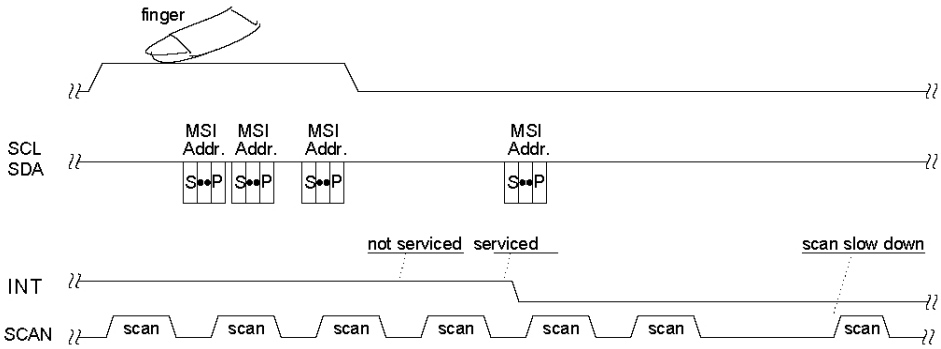


Figure 9.4.6: INT line will reset level when finger leaves and master has acknowledged the situation (INT_POL=1 in the INT mode register)

The only difference is send INT pulse instead of level between INT_ Mode=10 to INT_ Mode =11.

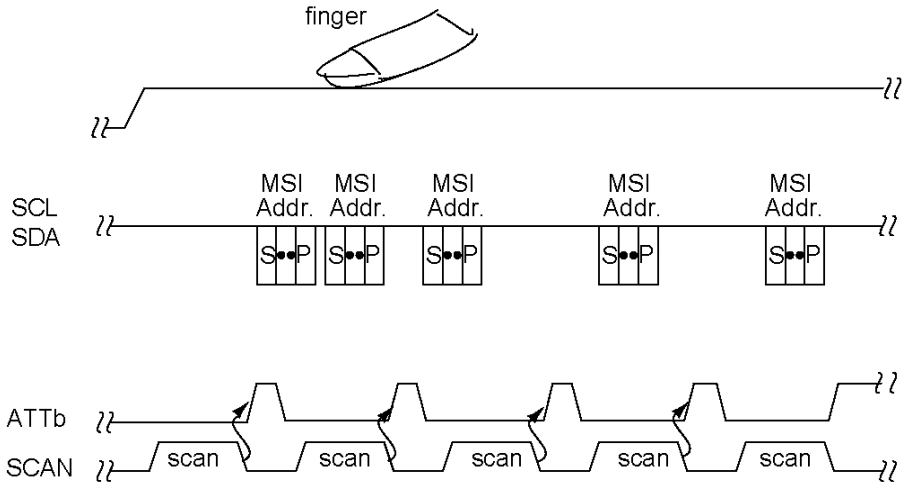


Figure 9.4.7: INT line pull up when finger touch (INT_POL=1, INT_MODE=11 in the INT mode register)

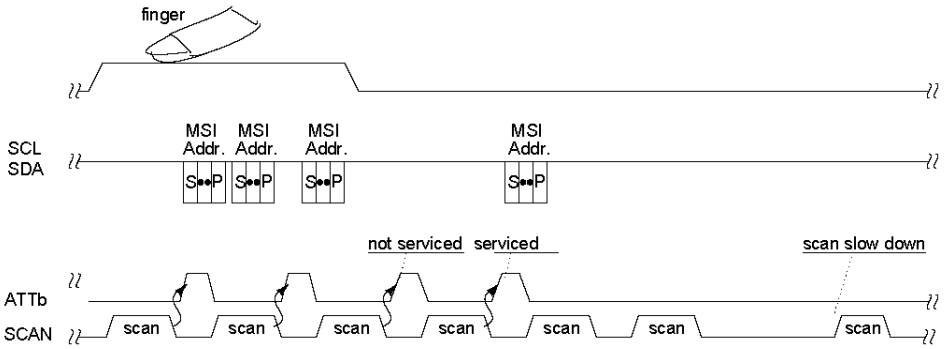
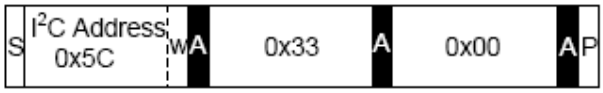


Figure 9.4.8: INT line will stop pulse when finger leaves and master has acknowledged the situation (INT_POL=1 in the INT mode register)

9.4.6 Power management

Active mode

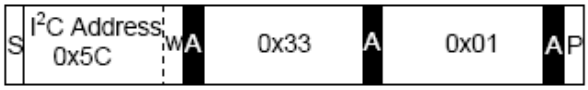
In this mode, the slave resumes with a new scan directly after each I^2C transfer (after INT rising edge). This is used to reach the highest refresh rate (reach to 400Hz), but also has the highest current consumption. Below is shows how to force the slave into Active mode.



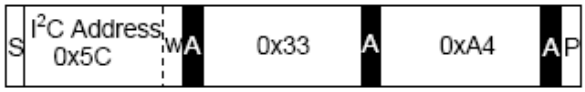
Active mode sequence

Sleep mode

This mode is selected to decrease the current consumption during low activity phases on the sensor, which need a lower refresh rate (10Hz or can be controlled by **Sleep_ freq** in table 9.4.2). The controller does automatically switch to Active mode when finger is detected or by setting the POWER_MODE register to Active mode. Also, the controller can automatically switch from Active to Sleep mode when no finger is detected for more than IDLE_PERIOD time, provided that ALLOW_SLEEP bit is set in the POWER_MODE register. Below are shows how to force the slave into Sleep mode and force the slave to switch automatically into Sleep mode (set ALLOW_SLEEP bit in POWER_MODE register).



Sleep mode sequence



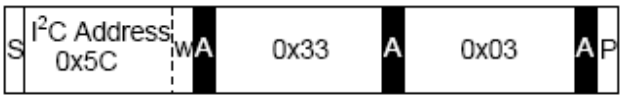
Sleep mode automatically switch sequence

Freeze mode

In this mode, the slave MCU internal clock source is stopped, and consumption is only MOS leakage.

Below shows how to force the slave into Freeze mode. There are two ways to wake up from freeze mode.

- RST pin pull down (connect to the Ground) (default)
- INT pin change (“1 to 0” or “0 to 1”)

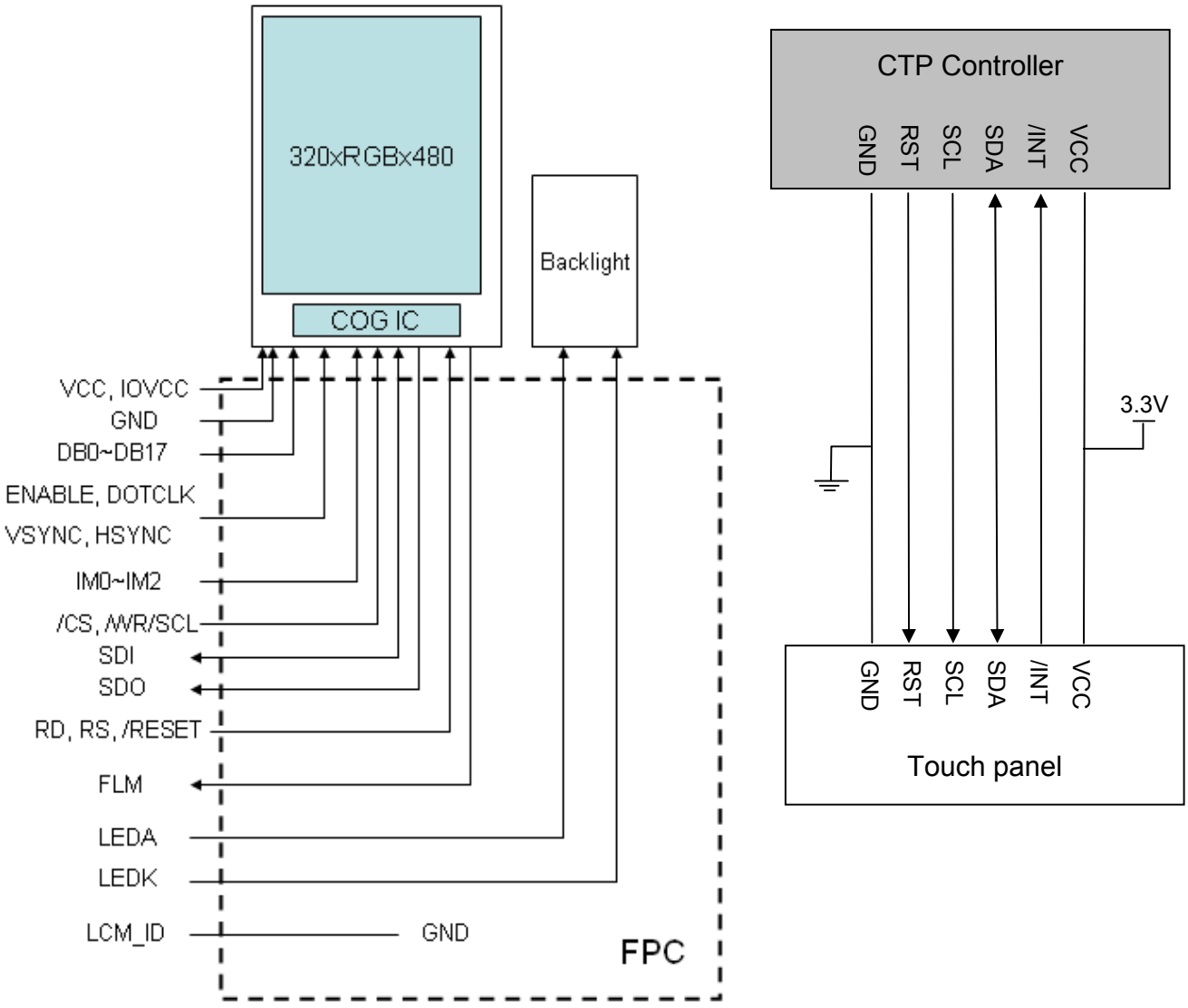


Freeze mode sequence

9.5 PIN CONNECTIONS

No.	Name	I/O	Description
1	VCC	-	Power
2	/INT	O	Interrupt output ,active Low
3	SDA	I/O	I²C data signal
4	SCL	I	I²C clock input
5	RST	I	Reset input , active High
6	GND	-	Ground
7	GND		
8	GND		

10. BLOCK DIAGRAM



11. QUALITY ASSURANCE

11.1 Test Condition

11.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 25 ± 5°C

Humidity : 65 ± 5%

11.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

11.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

11.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

11.1.5 Test Method

Reliability Test Item & Level		Test Level
No.	Test Item	
1	High Temperature Storage Test	T=80,240hrs
2	Low Temperature Storage Test	T=-30,240hrs
3	High Temperature Operation Test	T=70,240hrs
4	Low Temperature Operation Test	T=-20,240hrs
5	High Temperature and High Humidity (No operation)	T=60℃,90%RH,240hrs
6	Thermal Cycling Test (No operation)	-30℃ → +25℃ → +80℃, 100 Cycles 30 min 5 min 30 min
7	Vibration Test (No operation)	Frequency :10 ~ 55 H_Z Amplitude :1.5 mm Sweep time : 11 mins Test Period: 6 Cycles for each direction of X, Y, Z

11.2 Judgment standard

The Judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defect.

12. APPEARANCE SPECIFICATION

12.1 Inspection condition

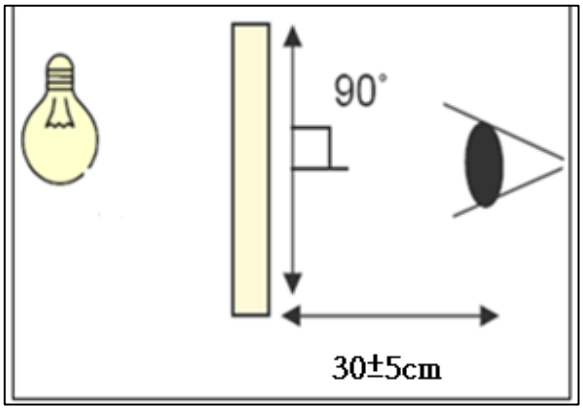
12.1.1 Inspection conditions

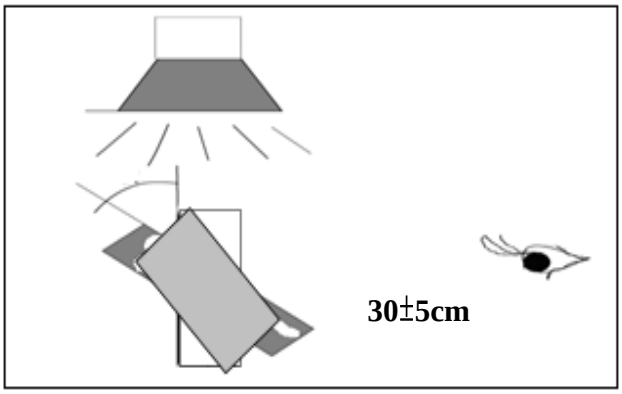
12.1.1.1 Inspection Distance : 30 ± 5 cm

12.1.1.2 View Angle :

(1) Inspection that light pervious to the product: 90±15°

(2) Inspection that light reflects on the product: 90±15°



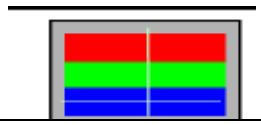


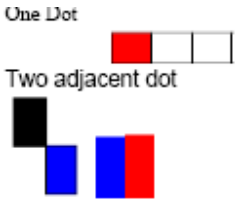
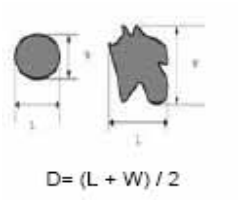
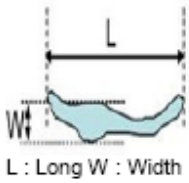
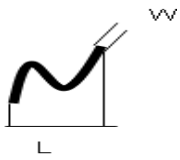
12.1.2 Environment conditions:

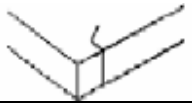
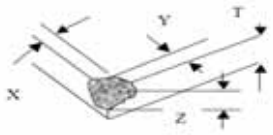
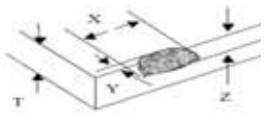
Ambient Temperature :	25±5℃
Ambient Humidity :	30~75%RH
Ambient Illumination	600~800 lux

12.2 Inspection Parameters

Appearance inspection standard (D: diameter, L: length; W: width, Z: height, T: glass thickness)

Inspection item	Inspection standard	Description
No image	Prohibited	
Image abnormal	Prohibited	
Bright line	Prohibited	
Thin line	It is acceptable that the defect can not be seen with 10% ND filter.	
Mura	It is acceptable that the defect can not be seen with 5% ND filter.	

<table>
<tr>
<td>Dot</td>
<td>
<table>
<tr><th rowspan="2">Item</th><th>Acceptable</th><th rowspan="2">Total</th></tr>
<tr><th>Visible area</th></tr>
<tr><td>Bright dot</td><td>2</td><td rowspan="2">5</td></tr>
<tr><td>Dark dot</td><td>4</td></tr>
<tr><td>Bright adjacent dots</td><td>1</td><td>1</td></tr>
<tr><td>Dark adjacent dots</td><td>2</td><td>2</td></tr>
<tr><td>Adjacent dots with a bright dot and a dark dot</td><td>1</td><td>1</td></tr>
</table>
</td>
<td> 
</td>
</tr>
<tr>
<td>Foreign material in dot shape</td>
<td>
<table>
<tr><th>SPEC (unit: mm)</th><th>Acceptable</th></tr>
<tr><td>D≦0.3</td><td>Ignored</td></tr>
<tr><td>0.3<D≦0.5, distance>5</td><td>n≦5</td></tr>
<tr><td>D＞0.5</td><td>0</td></tr>
</table>
</td>
<td> 
</td>
</tr>
<tr>
<td>Inspection item</td>
<td>Inspection standard</td>
<td>Description</td>
</tr>
<tr>
<td>Foreign material in line shape</td>
<td>
<table>
<tr><th>SPEC</th><th>Acceptable</th></tr>
<tr><td>W≦0.05 and L≦7</td><td>Ignored</td></tr>
<tr><td>0.05<W≦0.1, L≦7, distance >5</td><td>n≦5</td></tr>
<tr><td>W>0.1 or　L>7</td><td>0</td></tr>
</table>
</td>
<td> 
</td>
</tr>
<tr>
<td>Contamination</td>
<td>It is acceptable if the dirt can be wiped.</td>
<td></td>
</tr>
<tr>
<td>Inspection item</td>
<td>SPEC</td>
<td>Description</td>
</tr>
<tr>
<td>Scratch</td>
<td>
<table>
<tr><th>SPEC</th><th>Acceptable</th></tr>
<tr><td>W≦0.05 and L≦7</td><td>Ignored</td></tr>
<tr><td>0.05<W≦0.08, L≦7, distance >5</td><td>n≦5</td></tr>
<tr><td>0.08<W≦0.1, L≦7, distance >5</td><td>n≦3</td></tr>
<tr><td>W>0.1 or　L>7</td><td>0</td></tr>
</table>
</td>
<td> 
</td>
</tr>
</table>

<table>
<tr><td>Bubble</td><td><table><tr><td>SPEC (unit: mm)</td><td>Acceptable</td></tr><tr><td>D≦0.2</td><td>Ignored</td></tr><tr><td>Non visible area</td><td>Ignored</td></tr><tr><td>0.2<D≦0.3, distance >5</td><td>n≦5</td></tr><tr><td>D＞0.3</td><td>0</td></tr></table></td><td>  </td></tr>
<tr><td>Cover & Sensor Crack</td><td>Prohibited</td><td>  </td></tr>
<tr><td>Cover angle missing</td><td><table><tr><td>SPEC (unit: mm)</td><td>Acceptable</td></tr><tr><td>Side/Bottom</td><td>Ignored</td></tr><tr><td>It is prohibited if the defect appears on the front.</td><td>0</td></tr></table></td><td>  </td></tr>
<tr><td>Cover edge break</td><td><table><tr><td>SPEC (unit: mm)</td><td>Acceptable</td></tr><tr><td>X≦ 2.0, Y≦2.0, Z≦1/2T</td><td>Ignored</td></tr><tr><td>X>2.0, Y>2.0, Z＞1/2T</td><td>0</td></tr></table></td><td>  </td></tr>
<tr><td>Inspection item</td><td>SPEC</td><td>Description</td></tr>
<tr><td>Ink</td><td><table><tr><td>SPEC (unit: mm)</td><td>Acceptable</td></tr><tr><td>word unclear, inverted, mistake, break line</td><td>0</td></tr></table></td><td></td></tr>
<tr><td>Bubble under protection film</td><td><table><tr><td>SPEC (unit: mm)</td><td>Acceptable</td></tr><tr><td>NA</td><td></td></tr></table></td><td></td></tr>
<tr><td>Function</td><td>Prohibited</td><td></td></tr>
</table>

12.3 Sampling Condition

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.

Lot size: Quantity of shipment lot per model.

Sampling type: normal inspection, single sampling

Sampling table: MIL-STD-105E

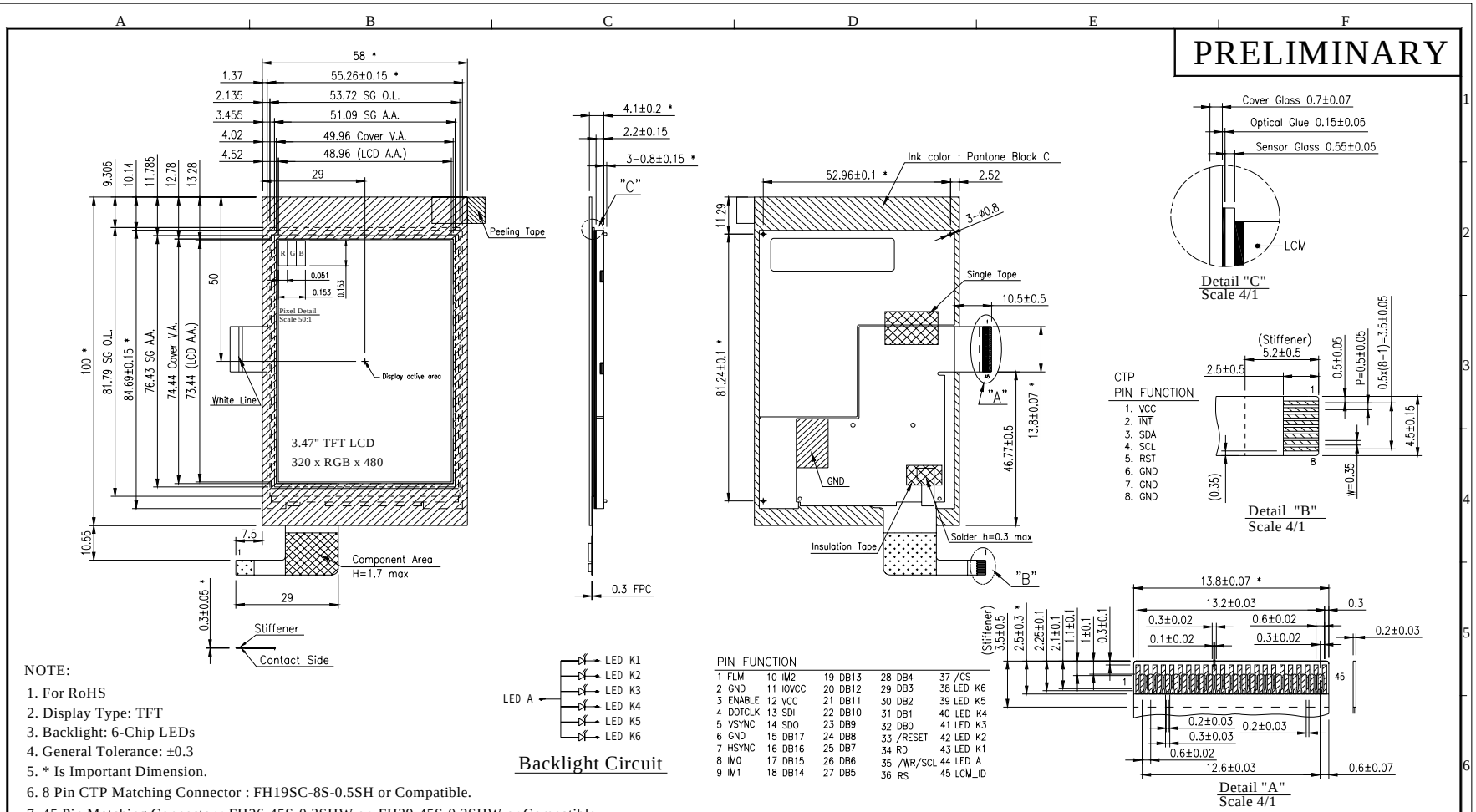
Inspection level: Level II

	Definition		
Class of defects	**Major**	AQL 0.65%	It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.
	Minor	AQL 1.5%	It is a defect that will not result in functioning problem with deviation classified.

13. PRECAUTIONS IN USE LCM

1. ASSEMBLY PRECAUTIONS
   (1) You must mount a module using holes arranged in four corners or four sides.
   (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
   (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
   (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
   (5) Do not open the case because inside circuits do not have sufficient strength.
   (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
   (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
   (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
2. OPERATING PRECAUTIONS
   (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
   (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
   (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
   (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
   (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
   (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
3. ELECTROSTATIC DISCHARGE CONTROL
   (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.
   (1) The modules should be kept in antistatic bags or other containers resistant to static for storage.
   (2) Only properly grounded soldering irons should be used.
   (3) If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
   (4) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
   (5) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.
4. STORAGE PRECAUTIONS
   (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
   (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
   (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
5. OTHERS
   (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
   (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
   (3) For the packaging box, please pay attention to the followings:
      a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
      b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
      c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

14. OUTLINE DRAWING



NOTE:

1. For RoHS
2. Display Type: TFT
3. Backlight: 6-Chip LEDs
4. General Tolerance: ±0.3
5. * Is Important Dimension.
6. 8 Pin CTP Matching Connector : FH19SC-8S-0.5SH or Compatible.
7. 45 Pin Matching Connector : FH26-45S-0.3SHW or FH39-45S-0.3SHW or Compatible.

AUTH	DESCRIPTION	DATE	APPROVED

REVISIONS

DATE:	
DRAWN:	
CHECK:	
APPROVE:	

TITLE:	LMTD2035CHN1-GCD1 3.5" CTP MODULE		
DWG. NO.	LMTD2035CHN1-GCD1		INTELTRONIC INC.
UNITS M M		REV. 1	
SCALE 1 / 1	SHEET 1 OF 1		

15 .Inspection Specifications

The buyer (customer) shall inspect the modules within twenty calendar days since the delivery date (the "inspection period") at its own cost. The results of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to the seller.

The buyer may, under commercially reasonable reject procedures, reject an entire lot in the delivery involved if, within the inspection period, such samples of modules within such lot show an unacceptable number of defects in accordance with this incoming inspection standards, provided however that the buyer must notify the seller in writing of any such rejection promptly, and not later than within three business days of the end of the inspection period.

Should the buyer fail to notify the seller within the inspection period, the buyer's right to reject the modules shall be lapsed and the modules shall be deemed to have been accepted by the buyer.

16. Warranty

Inteltronic Inc. warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for one year from the date of purchase.

Inteltronic Inc. will be limited to replace or repair any of its module which is found and confirmed defective electrically or visually when inspected in accordance with Inteltronic Inc. general module inspection standard.

This warranty does not apply to any products which have been on customer’s production line, repaired or altered by persons other than repair personnel authorized by Inteltronic Inc., or which have been subject to misuse, abuse, accident or improper installation. Inteltronic Inc. assumes no liability under the terms of this warranty as a consequence of such events.

If an Inteltronic Inc. product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. In returning the modules, they must be properly packaged with original package; there should be detailed description of the failures or defect.

17. RMA

Products purchased through Inteltronic Inc. and under warranty may be returned for replacement. Contact support@inteltronicinc.com for RMA number and procedures

Office Locations

INTELTRONIC

Inteltronic Inc.
www.inteltronicinc.com
Office: 510-471-9900
Fax: 510-471-9901
Address: 29470 Union City Blvd
Union City, CA 94587

www.wahlee.com
Wah Lee Industrial Corp.
HSINCHU OFFICE
18F, No.8, Zihciang S. Rd., Jhubei,
Hsinchu 302, Taiwan, R.O.C.
Tel : 886-3-6205880
FAX: 886-3-6205833