# 4.97 inch AMOLED
# SPECIFICATION
# MODEL NAME: LETB2050ZXN1

Date: 2015 / 10 / 6

| Customer Signature | | |
|---|---|---|
| Customer<br><br>Approved Date | Approved By | Reviewed By |
| | | |

## Record of Revision

| Version | Revise Date | Page | Content |
|---|---|---|---|
| 0. 0 | Feb. 28, 2015 | | First Draft |
| 0. 1 | May. 19, 2015 | 17 ,18 | Mo dif ied O LED Power Sup ply |
| | | 28 | Mo dif ied init ial c od e |
| | | 31 | Modified viewing angle CR, cross talk discription |
| | | 35 | Modified low temperature Spec |
| | Jun. 08, 2015 | 18 | Modified Power. |
| | Jun. 10, 2015 | 32 | Modified precaution. |
| 0.2 | Oct. 06, 2015 | 17~18 | Modified EE condition, added FPC bonding rules |
| | | 25 | Modified initial code |
| | | 27 | Modified Optical Specifications |
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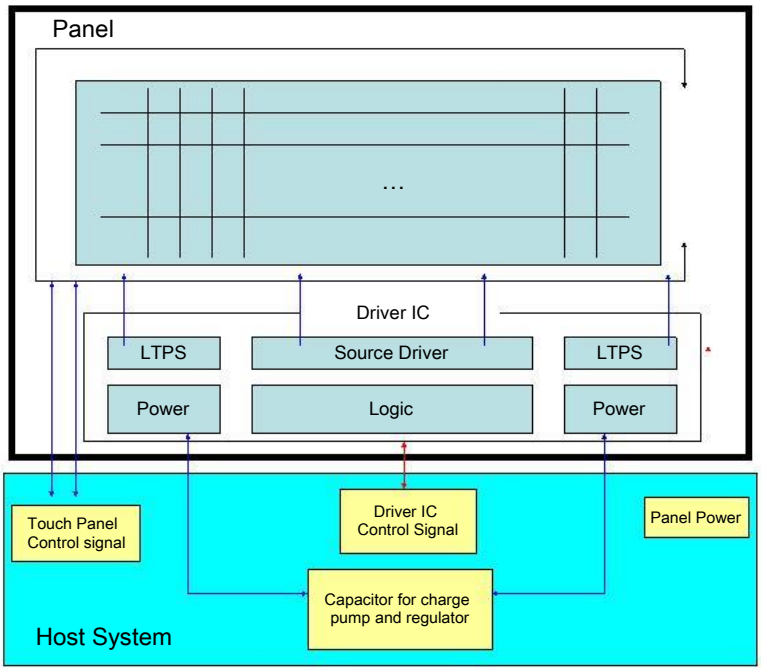
# Contents

# A. General Specification

## 1. AMOELD Panel Physical Specifications

| No. | Item | Spec. | Remark |
|---|---|---|---|
| 1 | Screen Size (inch) | 4.97” | |
| 2 | Display Resolution (dot) | 720xRGBx1280 | |
| 3 | Active Area (mm) | 61.92 (H)×110.08(V) | |
| 4 | Pixel Configuration | Real R.G.B | |
| 5 | Display Color | 16.7M | |
| 6 | Interface | MIPI DSI | VIDEO mode |
| 7 | Outline Dimension (mm) | 65.92 (H) × 118.64(V) × 0.77(T) | AMOLED w/ on-cell touch function |
| 8 | Suggested Touch IC | S3402 | Synaptics |
| 9 | Multi-Finger Touch | 10 | |

## 2. Suggested Module Composition



3. Main FPC fan-out pin assignment

AMOLED Panel Input/Output Signal Interface

| No. | Pin Assignment | IO | Discription | Remark |
|---|---|---|---|---|
| 1 | DUMMY_01 | - | NC | |
| 2 | OVSS_01 | Power | Panel Negative Voltage | |
| 3 | OVSS_02 | Power | Panel Negative Voltage | |
| 4 | OVSS_03 | Power | Panel Negative Voltage | |
| 5 | OVSS_04 | Power | Panel Negative Voltage | |
| 6 | OVSS_05 | Power | Panel Negative Voltage | |
| 7 | OVSS_06 | Power | Panel Negative Voltage | |
| 8 | OVSS_07 | Power | Panel Negative Voltage | |
| 9 | OVSS_08 | Power | Panel Negative Voltage | |
| 10 | DUMMY_02 | - | NC | |
| 11 | OVDD_01 | Power | Panel Positive Voltage | |
| 12 | OVDD_02 | Power | Panel Positive Voltage | |
| 13 | OVDD_03 | Power | Panel Positive Voltage | |
| 14 | OVDD_04 | Power | Panel Positive Voltage | |
| 15 | OVDD_05 | Power | Panel Positive Voltage | |
| 16 | OVDD_06 | Power | Panel Positive Voltage | |
| 17 | OVDD_07 | Power | Panel Positive Voltage | |
| 18 | OVDD_08 | Power | Panel Positive Voltage | |
| 19 | OVDD_09 | Power | Panel Positive Voltage | |
| 20 | OVDD_10 | Power | Panel Positive Voltage | |
| 21 | OVDD_11 | Power | Panel Positive Voltage | |
| 22 | DUMMY_03 | - | NC | |
| 23 | DVSS02 | Power | GND | |
| 24 | DVSS03 | Power | GND | |
| 25 | DVSS04 | Power | GND | |
| 26 | DVSS05 | Power | GND | |
| 27 | DVSS06 | Power | GND | |
| 28 | DVSS07 | Power | GND | |
| 29 | DVSS08 | Power | GND | |
| 30 | DVSS09 | Power | GND | |
| 31 | DVSS10 | Power | GND | |
| 32 | DVDD01 | O | IC internal regulator Output | |
| 33 | DVDD02 | O | IC internal regulator Output | |
| 34 | DVDD03 | O | IC internal regulator Output | |
| 35 | DVDD04 | O | IC internal regulator Output | |
| 36 | VREFN5 | O | IC internal regulator Output | |

| | | | | |
|---|---|---|---|---|
| 37 | VREFN | O | IC internal regulator Output | |
| 38 | VREFN10 | - | NC | Note 2 |
| 39 | VREFP5 | - | NC | |
| 40 | VREFP | - | NC | |
| 41 | VREFP10 | - | NC | |
| 42 | AVDD01 | O | Driver IC regulator Output | |
| 43 | AVDD02 | O | Driver IC regulator Output | |
| 44 | AVDD03 | O | Driver IC regulator Output | |
| 45 | AVSS01 | Power | GND | |
| 46 | AVSS02 | Power | GND | |
| 47 | AVSS03 | Power | GND | |
| 48 | VGLR_01 | O | Driver IC regulator Output | |
| 49 | VGLR2_01 | O | Driver IC regulator Output | |
| 50 | VGHR_01 | O | Driver IC regulator Output | |
| 51 | VGHR2_01 | O | Driver IC regulator Output | |
| 52 | MTP_PWR1 | O | NC | Note 3 |
| 53 | MTP_PWR2 | O | NC | |
| 54 | D3_P1 | O | NC | Note 2 |
| 55 | D3_P2 | O | NC | |
| 56 | VSS3D01 | Power | GND | |
| 57 | BVP3D01 | O | NC | Note 2 |
| 58 | BVN3D01 | O | NC | |
| 59 | VGL_01 | O | Driver IC regulator Output | |
| 60 | VGH_01 | O | Driver IC regulator Output | |
| 61 | VCL_01 | O | Driver IC regulator Output | |
| 62 | VCL_02 | O | Driver IC regulator Output | |
| 63 | VCL_03 | O | Driver IC regulator Output | |
| 64 | VREF | O | Driver IC regulator Output | |
| 65 | VSSA | Power | GND | |
| 66 | VDDA | Power | Driver IC Analog Supply | |
| 67 | VDDR01 | Power | Driver IC Analog Supply | |
| 68 | VDDR02 | Power | Driver IC Analog Supply | |
| 69 | VSSR01 | Power | GND | |
| 70 | VSSR02 | Power | GND | |
| 71 | VDD_DET0 | Power | Driver IC Analog Supply | |
| 72 | VDD_DET1 | Power | Driver IC Analog Supply | |
| 73 | DIOPWR0 | O | NC | Note 2 |
| 74 | DIOPWR1 | O | NC | |
| 75 | VGSP | O | Driver IC regulator Output | |



| | | | | |
|---|---|---|---|---|
| 76 | VGMP | O | Driver IC regulator Output | |
| 77 | DVSS11 | Power | GND | |
| 78 | DVSS12 | Power | GND | |
| 79 | DVSS13 | Power | GND | |
| 80 | DVDD5 | O | Driver IC regulator Output | |
| 81 | DVDD6 | O | Driver IC regulator Output | |
| 82 | DVDD7 | O | Driver IC regulator Output | |
| 83 | AVSS04 | Power | GND | |
| 84 | AVSS05 | Power | GND | |
| 85 | VDDI_OPT1_1 | O | NC | Note 2 |
| 86 | LANSEL_0 | I | Connect to GND | MIPI 4 Data Lanes |
| 87 | LANSEL_1 | I | Connect to VDDI | |
| 88 | DSWAP_0 | I | Connect to GND | MIPI Data Lane Sequence |
| 89 | DSWAP_1 | I | Connect to VDDI | |
| 90 | PSWAP | I | Connect to GND | |
| 91 | DSTB_SEL | I | Connect to GND | |
| 92 | I2C_SA0 | I | Connect to GND | |
| 93 | IM3 | I | Connect to GND | MIPI DSI |
| 94 | IM2 | I | Connect to VDDI | |
| 95 | IM1 | I | Connect to GND | |
| 96 | IM0 | I | Connect to GND | |
| 97 | SWIRE | O | Power IC Control | Swire protocol setting pin of Power IC, If not used, please NC |
| 98 | OLED_EN | O | Power IC enable control pin, If not used, please NC | Power IC enable control pin, If not used, please NC |
| 99 | EXB1T | I | Connect to GND | Use IC Internal AVDD |
| 100 | TE_L | O | Note 4 | Note 4 |
| 101 | VSEL | I | Connect to GND | Note 1 |
| 102 | SDO | O | NC | Not used |
| 103 | SDI | I | Connect to GND | Note 1 |



| | | | | |
|---|---|---|---|---|
| 104 | DCX | I | Connect to GND | |
| 105 | WRX | I | Connect to GND | |
| 106 | RDX | I | Connect to GND | |
| 107 | CSX | I | Connect to GND | |
| 108 | RESX | I | This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. | |
| 109 | VSSI01 | Power | GND | |
| 110 | VSSI02 | Power | GND | |
| 111 | VDDI01 | Power | Digital power supply | |
| 112 | VDDI02 | Power | Digital power supply | |
| 113 | SCL_M | O | NC | Note 2 |
| 114 | SDA_M | I/O | NC | |
| 115 | MUX13 | O | Connect to GND | Note 1 |
| 116 | PMOS0 | I | Connect to VDDI | PMOS type |
| 117 | PMOS1 | I | Connect to GND | |
| 118 | CGM[2] | I | Connect to GND | Resolution Control Pin |
| 119 | CGM[1] | I | Connect to VDDI | |
| 120 | CGM[0] | I | Connect to GND | |
| 121 | D23 | O | Connect to GND | Note 1 |
| 122 | D22 | O | Connect to GND | |
| 123 | D21 | O | Connect to GND | |
| 124 | D20 | O | Connect to GND | |
| 125 | D19 | O | Connect to GND | |
| 126 | D18 | O | Connect to GND | |
| 127 | D17 | O | Connect to GND | |
| 128 | D16 | O | Connect to GND | |
| 129 | D15 | O | Connect to GND | |
| 130 | D14 | O | Connect to GND | |
| 131 | D13 | O | Connect to GND | |
| 132 | D12 | O | Connect to GND | |
| 133 | D11 | O | Connect to GND | |
| 134 | D10 | O | Connect to GND | |
| 135 | D09 | O | Connect to GND | |
| 136 | D08 | O | Connect to GND | |
| 137 | D07 | O | Connect to GND | |
| 138 | D06 | O | Connect to GND | |
| 139 | D05 | O | Connect to GND | |



| | | | | |
|---|---|---|---|---|
| 140 | D04 | O | Connect to GND | |
| 141 | D03 | O | Connect to GND | |
| 142 | D02 | O | Connect to GND | |
| 143 | D01 | O | Connect to GND | |
| 144 | D00 | O | Connect to GND | |
| 145 | PCLK | O | Connect to GND | |
| 146 | DE | O | Connect to GND | |
| 147 | HS | O | Connect to GND | |
| 148 | VS | O | Connect to GND | |
| 149 | ERR | O | NC | Note 3 |
| 150 | VDDI03 | Power | Digital power supply | |
| 151 | VDDI04 | Power | Digital power supply | |
| 152 | VSSI03 | Power | GND | |
| 153 | VSSI04 | Power | GND | |
| 154 | VDDA2 | Power | Driver IC Analog Supply | |
| 155 | VDDA3 | Power | Driver IC Analog Supply | |
| 156 | VDDA4 | Power | Driver IC Analog Supply | |
| 157 | AVDD07 | O | Driver IC regulator Output | |
| 158 | AVDD04 | O | Driver IC regulator Output | |
| 159 | AVDD05 | O | Driver IC regulator Output | |
| 160 | AVDD06 | O | Driver IC regulator Output | |
| 161 | AVEE1 | O | Driver IC regulator Output | |
| 162 | AVEE2 | O | Driver IC regulator Output | |
| 163 | DVSS14 | Power | GND | |
| 164 | DVSS15 | Power | GND | |
| 165 | DVSS16 | Power | GND | |
| 166 | DVDD08 | O | Driver IC regulator Output | |
| 167 | DVDD09 | O | Driver IC regulator Output | |
| 168 | DVDD10 | O | Driver IC regulator Output | |
| 169 | DVDD11 | O | Driver IC regulator Output | |
| 170 | MVDDA1 | O | Driver IC regulator Output | |
| 171 | MVDDA2 | O | Driver IC regulator Output | |
| 172 | VDDAM02 | Power | Driver IC Analog Supply | |
| 173 | VDDAM03 | Power | Driver IC Analog Supply | |
| 174 | MVDDL1 | O | Driver IC regulator Output | |
| 175 | MVDDL2 | O | Driver IC regulator Output | |
| 176 | VSSAM04 | Power | GND | |
| 177 | HSSI_D3_P1 | I | MIPI DSI data2+ | |
| 178 | HSSI_D3_P2 | I | MIPI DSI data2+ | |

| | | | | |
|---|---|---|---|---|
| 179 | HSSI_D3_N1 | I | MIPI DSI data2- | |
| 180 | HSSI_D3_N2 | I | MIPI DSI data2- | |
| 181 | VSSAM05 | Power | GND | |
| 182 | VSSAM06 | Power | GND | |
| 183 | HSSI_D1_P1 | I | MIPI DSI data1+ | |
| 184 | HSSI_D1_P2 | I | MIPI DSI data1+ | |
| 185 | HSSI_D1_N1 | I | MIPI DSI data1- | |
| 186 | HSSI_D1_N2 | I | MIPI DSI data1- | |
| 187 | VSSAM07 | Power | GND | |
| 188 | VSSAM08 | Power | GND | |
| 189 | HSSI_CLK_P1 | I | MIPI DSI clock+ | |
| 190 | HSSI_CLK_P2 | I | MIPI DSI clock+ | |
| 191 | HSSI_CLK_N1 | I | MIPI DSI clock- | |
| 192 | HSSI_CLK_N2 | I | MIPI DSI clock- | |
| 193 | VSSAM09 | Power | GND | |
| 194 | VSSAM10 | Power | GND | |
| 195 | HSSI_D0_P1 | I/O | MIPI DSI data0+ | |
| 196 | HSSI_D0_P2 | I/O | MIPI DSI data0+ | |
| 197 | HSSI_D0_N1 | I/O | MIPI DSI data0- | |
| 198 | HSSI_D0_N2 | I/O | MIPI DSI data0- | |
| 199 | VSSAM11 | Power | GND | |
| 200 | VSSAM12 | Power | GND | |
| 201 | HSSI_D2_P1 | I | MIPI DSI data3+ | |
| 202 | HSSI_D2_P2 | I | MIPI DSI data3+ | |
| 203 | HSSI_D2_N1 | I | MIPI DSI data3- | |
| 204 | HSSI_D2_N2 | I | MIPI DSI data3- | |
| 205 | VSSAM13 | Power | GND | |
| 206 | VSSAM14 | Power | GND | |
| 207 | VDDR03 | Power | Driver IC Analog Supply | |
| 208 | Analog_Test | - | NC | Note 3 |
| 209 | TE_R | O | NC | Note 4 |
| 210 | VSSR | Power | GND | |
| 211 | VREFCP | O | Driver IC regulator Output | |
| 212 | VGHR | O | Driver IC regulator Output | |
| 213 | EXTP01 | - | NC | Note 2 |
| 214 | EXTP02 | - | NC | |
| 215 | CSP01 | - | NC | |
| 216 | CSP02 | - | NC | |
| 217 | EXTN01 | - | NC | |



| | | | | |
|---|---|---|---|---|
| 218 | EXTN02 | - | NC | |
| 219 | CSN01 | - | NC | |
| 220 | CSN02 | - | NC | |
| 221 | AVSS08 | Power | GND | |
| 222 | AVSS06 | Power | GND | |
| 223 | AVSS07 | Power | GND | |
| 224 | C18N01 | I/O | Charge pump Capacitor | |
| 225 | C18N02 | I/O | | |
| 226 | C18N03 | I/O | | |
| 227 | C18P01 | I/O | | |
| 228 | C18P02 | I/O | | |
| 229 | C18P03 | I/O | | |
| 230 | C17N01 | I/O | Charge pump Capacitor | |
| 231 | C17N02 | I/O | | |
| 232 | C17P01 | I/O | | |
| 233 | C17P02 | I/O | | |
| 234 | C16N01 | I/O | Charge pump Capacitor | |
| 235 | C16N02 | I/O | | |
| 236 | C16N03 | I/O | | |
| 237 | C16P01 | I/O | | |
| 238 | C16P02 | I/O | | |
| 239 | C16P03 | I/O | | |
| 240 | C15N01 | I/O | Charge pump Capacitor | |
| 241 | C15N02 | I/O | | |
| 242 | C15N03 | I/O | | |
| 243 | C15P01 | I/O | | |
| 244 | C15P02 | I/O | | |
| 245 | C15P03 | I/O | | |
| 246 | AVDD12 | O | Driver IC regulator Output | |
| 247 | AVDD13 | O | Driver IC regulator Output | |
| 248 | AVDD8 | O | Driver IC regulator Output | |
| 249 | AVDD9 | O | Driver IC regulator Output | |
| 250 | AVDD10 | O | Driver IC regulator Output | |
| 251 | AVDD11 | O | Driver IC regulator Output | |
| 252 | VDDB1 | Power | Driver IC Analog Supply | |
| 253 | VDDB2 | Power | Driver IC Analog Supply | |
| 254 | VDDB3 | Power | Driver IC Analog Supply | |
| 255 | VDDB4 | Power | Driver IC Analog Supply | |
| 256 | VDDB5 | Power | Driver IC Analog Supply | |

| | | | | |
|---|---|---|---|---|
| 257 | VSSB1 | Power | GND | |
| 258 | VSSB2 | Power | GND | |
| 259 | VSSB3 | Power | GND | |
| 260 | C11P01 | I/O | | |
| 261 | C11P02 | I/O | Charge pump Capacitor | |
| 262 | C11N01 | I/O | | |
| 263 | C11N02 | I/O | | |
| 264 | C12P01 | I/O | Charge pump Capacitor | |
| 265 | C12P02 | I/O | | |
| 266 | C12N01 | I/O | | |
| 267 | C12N02 | I/O | | |
| 268 | C13P01 | I/O | Charge pump Capacitor | |
| 269 | C13P02 | I/O | | |
| 270 | C13N01 | I/O | | |
| 271 | C13N02 | I/O | | |
| 272 | C14P01 | I/O | Charge pump Capacitor | |
| 273 | C14P02 | I/O | | |
| 274 | C14N01 | I/O | | |
| 275 | C14N02 | I/O | | |
| 276 | C14N03 | I/O | | |
| 277 | C31P01 | I/O | Charge pump Capacitor | |
| 278 | C31P02 | I/O | | |
| 279 | C31P03 | I/O | | |
| 280 | C31N01 | I/O | | |
| 281 | C31N02 | I/O | | |
| 282 | C32P01 | I/O | Charge pump Capacitor | |
| 283 | C32P02 | I/O | | |
| 284 | C32P03 | I/O | | |
| 285 | C32N01 | I/O | | |
| 286 | C32N02 | I/O | | |
| 287 | C32N03 | I/O | | |
| 288 | VCL04 | O | Driver IC regulator Output | |
| 289 | VCL05 | O | Driver IC regulator Output | |
| 290 | VCL06 | O | Driver IC regulator Output | |
| 291 | C21P01 | I/O | Charge pump Capacitor | |
| 292 | C21P02 | I/O | | |
| 293 | C21N01 | I/O | | |
| 294 | C21N02 | I/O | | |
| 295 | C22P01 | I/O | Charge pump Capacitor | |

| | | | | |
|---|---|---|---|---|
| 296 | C22P02 | I/O | Driver IC regulator Output | |
| 297 | C22N01 | I/O | | |
| 298 | C22N02 | I/O | | |
| 299 | AVEE3 | O | | |
| 300 | VDDB06 | Power | Driver IC Analog Supply | |
| 301 | VDDB07 | Power | Driver IC Analog Supply | |
| 302 | VDDB08 | Power | Driver IC Analog Supply | |
| 303 | VSSB04 | Power | GND | |
| 304 | VSSB05 | Power | GND | |
| 305 | C41P | I/O | Charge pump Capacitor | |
| 306 | C41N | I/O | | |
| 307 | C42P | I/O | Charge pump Capacitor | |
| 308 | C42N | I/O | | |
| 309 | C51P | I/O | Charge pump Capacitor | |
| 310 | C51N | I/O | | |
| 311 | C52P | I/O | Charge pump Capacitor | |
| 312 | C52N | I/O | | |
| 313 | VGH | O | Driver IC regulator Output | |
| 314 | VGL | O | Driver IC regulator Output | |
| 315 | VGHR2_02 | O | Driver IC regulator Output | |
| 316 | VGHR_02 | O | Driver IC regulator Output | |
| 317 | VGLR2_02 | O | Driver IC regulator Output | |
| 318 | VGLR_02 | O | Driver IC regulator Output | |
| 319 | AVSS11 | Power | GND | |
| 320 | AVSS09 | Power | GND | |
| 321 | AVSS10 | Power | GND | |
| 322 | AVDD15 | O | Driver IC regulator Output | |
| 323 | AVDD16 | O | Driver IC regulator Output | |
| 324 | AVDD14 | O | Driver IC regulator Output | |
| 325 | DVDD12 | O | Driver IC regulator Output | |
| 326 | DVDD13 | O | Driver IC regulator Output | |
| 327 | DVDD14 | O | Driver IC regulator Output | |
| 328 | DVDD15 | O | Driver IC regulator Output | |
| 329 | DVSS17 | Power | GND | |
| 330 | DVSS18 | Power | GND | |
| 331 | DVSS19 | Power | GND | |
| 332 | DVSS20 | Power | GND | |
| 333 | DVSS21 | Power | GND | |
| 334 | DVSS22 | Power | GND | |

| | | | | |
|---|---|---|---|---|
| 335 | DVSS23 | Power | GND | |
| 336 | DVSS24 | Power | GND | |
| 337 | DVSS25 | Power | GND | |
| 338 | DUMMY_05 | - | NC | |
| 339 | OVDD_12 | Power | Panel Positive Voltage | |
| 340 | OVDD_13 | Power | Panel Positive Voltage | |
| 341 | OVDD_14 | Power | Panel Positive Voltage | |
| 342 | OVDD_15 | Power | Panel Positive Voltage | |
| 343 | OVDD_16 | Power | Panel Positive Voltage | |
| 344 | OVDD_17 | Power | Panel Positive Voltage | |
| 345 | OVDD_18 | Power | Panel Positive Voltage | |
| 346 | OVDD_19 | Power | Panel Positive Voltage | |
| 347 | OVDD_20 | Power | Panel Positive Voltage | |
| 348 | OVDD_21 | Power | Panel Positive Voltage | |
| 349 | OVDD_22 | Power | Panel Positive Voltage | |
| 350 | DUMMY_06 | - | NC | |
| 351 | OVSS_09 | Power | Panel Negative Voltage | |
| 352 | OVSS_10 | Power | Panel Negative Voltage | |
| 353 | OVSS_11 | Power | Panel Negative Voltage | |
| 354 | OVSS_12 | Power | Panel Negative Voltage | |
| 355 | OVSS_13 | Power | Panel Negative Voltage | |
| 356 | OVSS_14 | Power | Panel Negative Voltage | |
| 357 | OVSS_15 | Power | Panel Negative Voltage | |
| 358 | OVSS_16 | Power | Panel Negative Voltage | |
| 359 | DUMMY_07 | - | NC | |

I:Input pin; O: Output pin; P:Power pin; NC: No connection n; I/O: In-out pin

Note 1: These pins are set for other Interface. To avoid interference, connect to GND

Note 2: These pins are not used in MIPI DSI interfance or panel control signal. No Connection

Note 3: Test pin, not accessible to user. Must be left open

Note 4: Tearing effect output pin to synchronize, TE_L is set output by default.



4. Touch FPC fan-out pin assignment

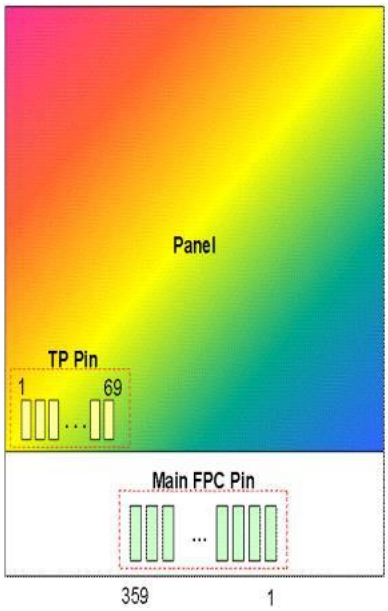
| FPC Pin No | Symbol |
|---|---|
| 1 | Dummy |
| 2 | Dummy |
| 3 | Dummy |
| 4 | GND |
| 5 | GND |
| 6 | Y14_TX3 |
| 7 | Y13_TX2 |
| 8 | Y12_TX1 |
| 9 | Y11 |
| 10 | Y10 |
| 11 | Y9 |
| 12 | Y8 |
| 13 | Y7 |
| 14 | Y6 |
| 15 | Y5 |
| 16 | Y4 |
| 17 | Y3 |
| 18 | Y2 |
| 19 | Y1 |
| 20 | Y0 |
| 21 | GND |
| 22 | Y0 |
| 23 | Y1 |

| FPC Pin No | Symbol |
|---|---|
| 24 | Y2 |
| 25 | Y3 |
| 26 | Y4 |
| 27 | Y5 |
| 28 | Y6 |
| 29 | Y7 |
| 30 | Y8 |
| 31 | Y9 |
| 32 | Y10 |
| 33 | Y11 |
| 34 | Y12_TX1 |
| 35 | Y13_TX2 |
| 36 | Y14_TX3 |
| 37 | GND |
| 38 | GND |
| 39 | X25 |
| 40 | X24 |
| 41 | X23 |
| 42 | X22 |
| 43 | X21 |
| 44 | X20 |
| 45 | X19 |
| 46 | X18 |

| FPC Pin No | Symbol |
|---|---|
| 47 | X17 |
| 48 | X16 |
| 49 | X15 |
| 50 | X14 |
| 51 | X13 |
| 52 | X12 |
| 53 | X11 |
| 54 | X10 |
| 55 | X9 |
| 56 | X8 |
| 57 | X7 |
| 58 | X6 |
| 59 | X5 |
| 60 | X4 |
| 61 | X3 |
| 62 | X2 |
| 63 | X1 |
| 64 | X0 |
| 65 | GND |
| 66 | GND |
| 67 | Dummy |
| 68 | Dummy |
| 69 | Dummy |

X – TP Rx, Y – TP Tx

## 5. Mechanical Schematic

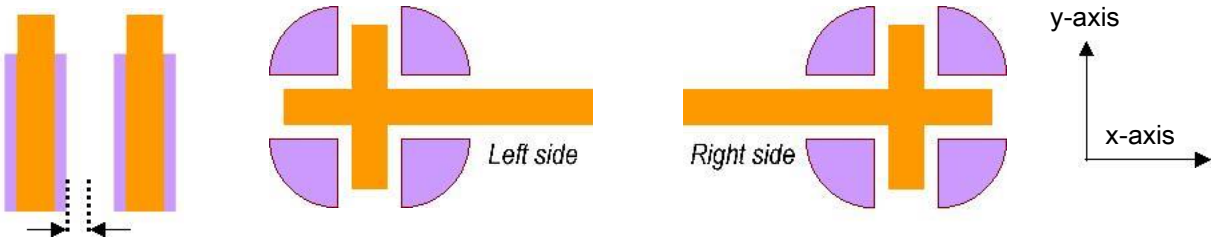



## 6. Absolute Maximum Ratings

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| OLED Power supply | OVDD | -- | +4.6 | V |
| | OVSS | -3.4 | -- | V |
| Digital Power supply | VDDI | -0.3 | +2.0 | V |
| Analog Power supply | VCI | -0.3 | +4.0 | V |

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently.

## 7. FPC Bonding Rules




x axis < ½ space (pad to pad)  y axis < ½ at ¼ of circle

| Measurement | Bonding Resistance |
|---|---|
| Power IC OVDD to Right OVDD E-pad | 1.5Ω |
| Power IC OVDD to Left OVDD E-pad | 2.0Ω |
| Power IC OVSS to Right OVSS E-pad | 3.5Ω |
| Power IC OVSS to Left OVSS E-pad | 3.5Ω |

## B. DC Characteristics

### 1. Operation Conditions

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| OLED Power supply | | OVDD | -- | +4.6 | -- | V | |
| | | OVSS | -- | -3.4 | -- | V | |
| Digital Power supply | | VDDI | 1.65 | 1.8 | 1.95 | V | |
| Analog Power supply | | VCI | 2.7 | 3.1 | 3.6 | V | |
| Input Signal Voltage | H Level | $V_{IH}$ | 0.8*VDDI | - | VDDI | V | RESX |
| | L Level | $V_{IL}$ | 0 | - | 0.2*VDDI | V | |
| Output Signal Voltage | H Level | $V_{OH}$ | 0.7*VDDI | - | VDDI | V | TE |
| | L Level | $V_{OL}$ | 0 | - | 0.3*VDDI | V | |

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

### 2. Display Current Consumption

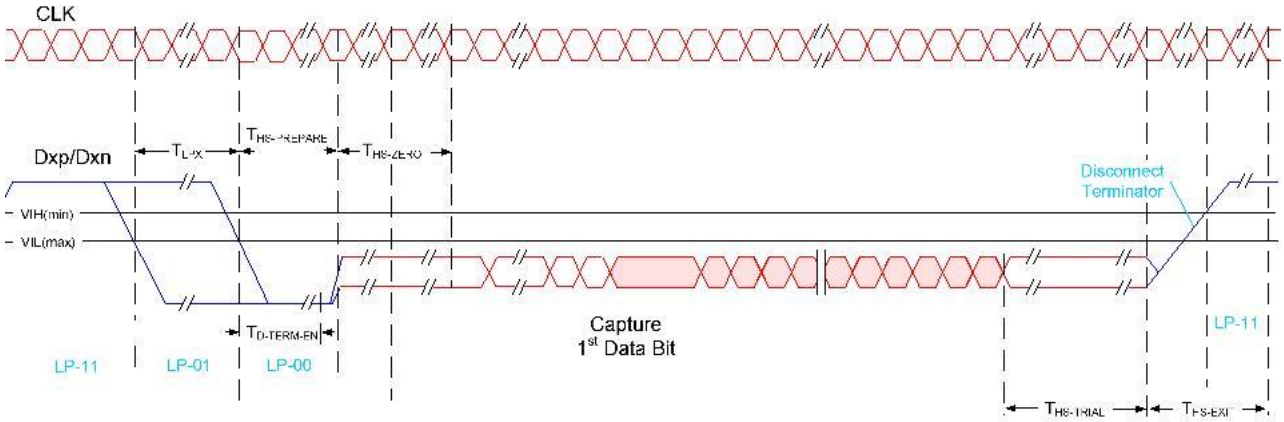
| Mode | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Normal | $I_{OVDD-OVSS}$ | OVDD = +4.6V<br>OVSS = -3.4 V<br>VCI = 3.1V<br>VDDI = 1.8V | - | 450 | 550 | mA |
| | $I_{VCI}$ | | - | 60 | 80 | mA |
| | $I_{VDDI}$ | | - | 1 | 10 | mA |
| Deep Standby (DSTB=1) | $I_{OVDD/OVSS}$ | | - | - | <1 | mA |
| | $I_{VCI}$ | | - | - | <1 | mA |
| | $I_{VDDI}$ | | - | - | <1 | μA |

Note 1: Based on white pattern. MIPI-DSI frame rate 60Hz video mode.
Note 2: Display off. RESX = high

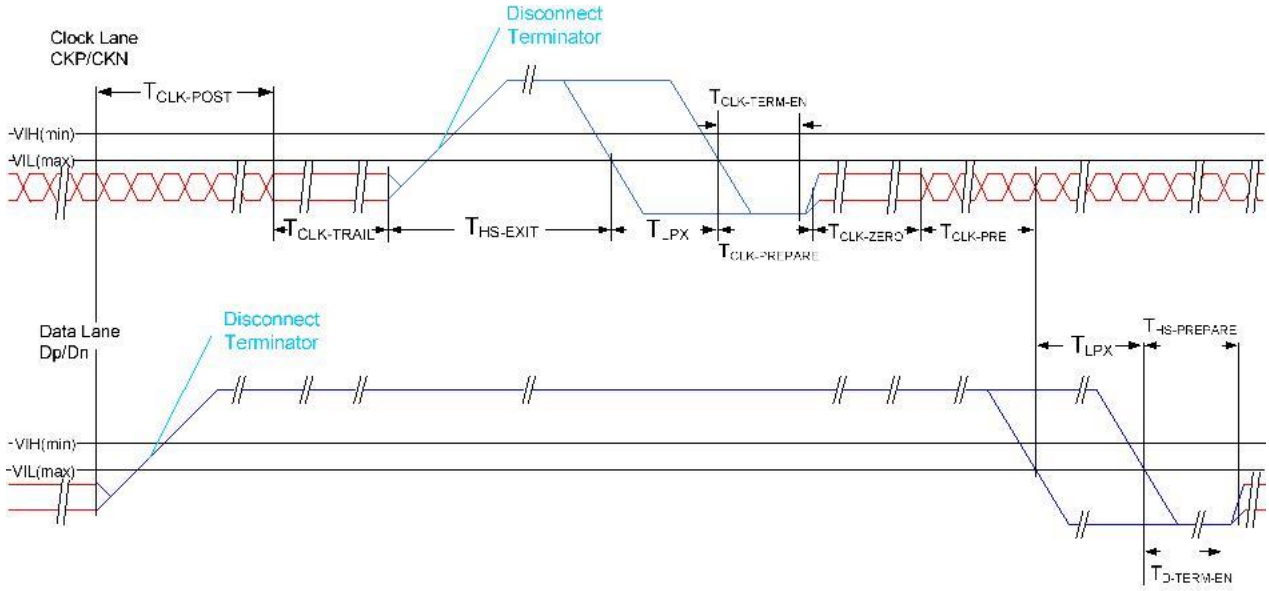
# C. AC Characteristics

## 1. Display AC Characteristics

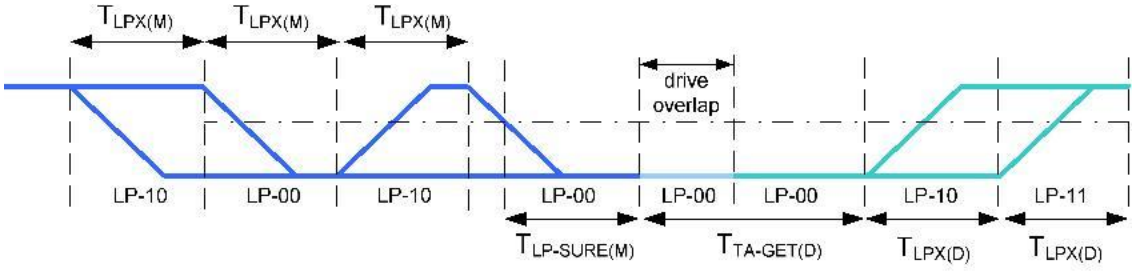
### HS Data Transmission Burst




### HS clock transmission




### Turnaround Procedure



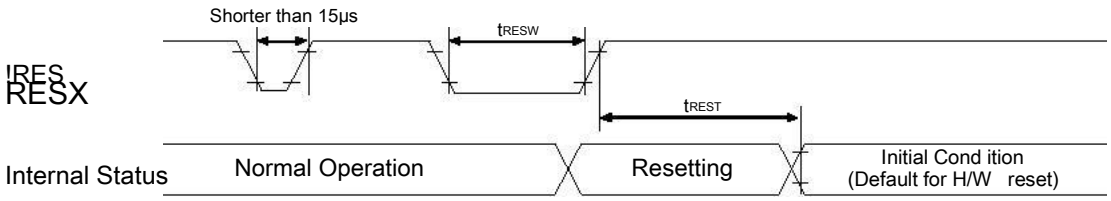
Timing Parameters

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$. | 60ns + 52*UI | | | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 300 | | | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | Time for Dn to reach $V_{TERM-EN}$ | | 38 | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | Time for Dn to reach $V_{TERM-EN}$ | | 35 ns +4*UI | |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4*UI | | 85 ns + 6*UI | ns |

| | | | | | |
|---|---|---|---|---|---|
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145ns + 10*UI | | | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60ns + 4*UI | | | ns |
| $T_{LPX(M)}$ | Transmitted length of any Low-Power state period of MCU to display module | 50 | | 150 | ns |
| $T_{TA-SURE(M)}$ | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(M)}$ | | 2*$T_{LPX(M)}$ | ns |
| $T_{LPX(D)}$<br>$T_{TA-GET(D)}$ | Transmitted length of any Low-Power state period of display module to MCU<br>Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | 50<br>5*$T_{LPX(D)}$ | | 150 | ns<br>ns |
| $T_{TA-GO(D)}$ | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | 4*$T_{LPX(D)}$ | | | ns |
| $T_{TA-SURE(D)}$ | Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(D)}$ | | 2*$T_{LPX(D)}$ | ns |

2. Display RESET Timing Characteristics

Reset input timing




Timing Parameters

| Symbol | Parameter | Related Pins | MIN | TYP | MAX | Note | Unit |
|---|---|---|---|---|---|---|---|
| tRESW | *1) Reset low pulse width | RESX | 15 | - | - | - | µs |
| tREST | *2) Reset complete time | - | - | - | 5 | When reset applied during Sleep in mode | ms |
| | | - | | - | 120 | When reset applied during Sleep out mode | ms |

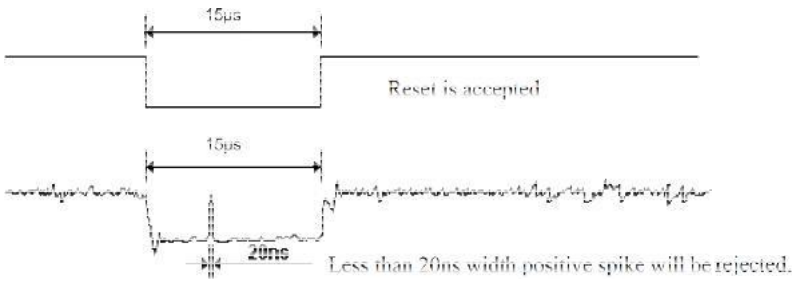
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5µs | Invalid Reset |
| Longer than 15µs | Valid Reset |
| Between 5µs and 15µs | Reset Initialization Precedure |

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

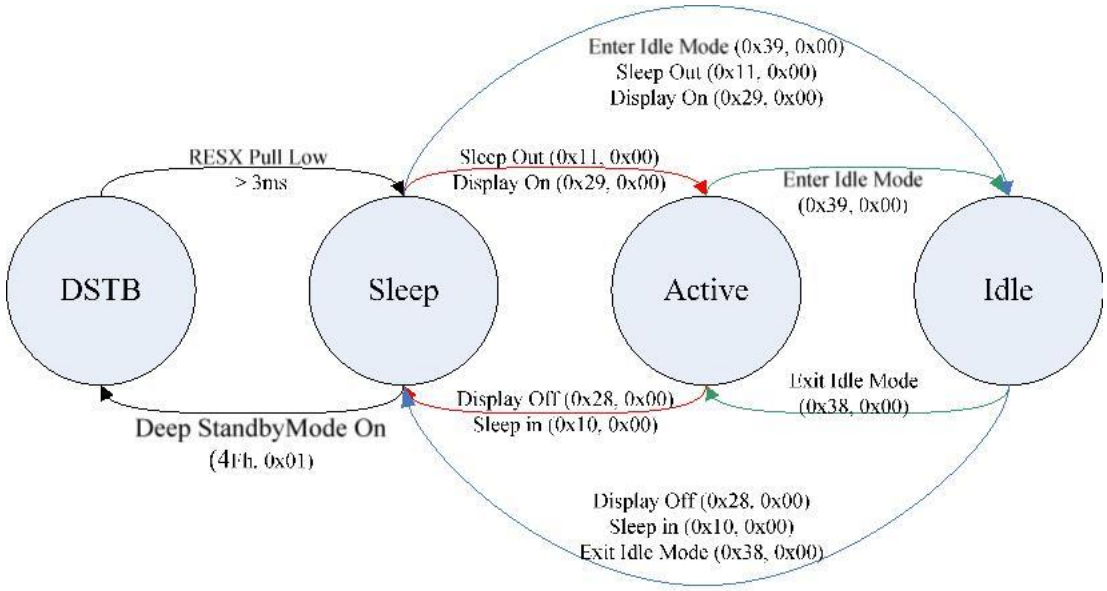
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:




Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

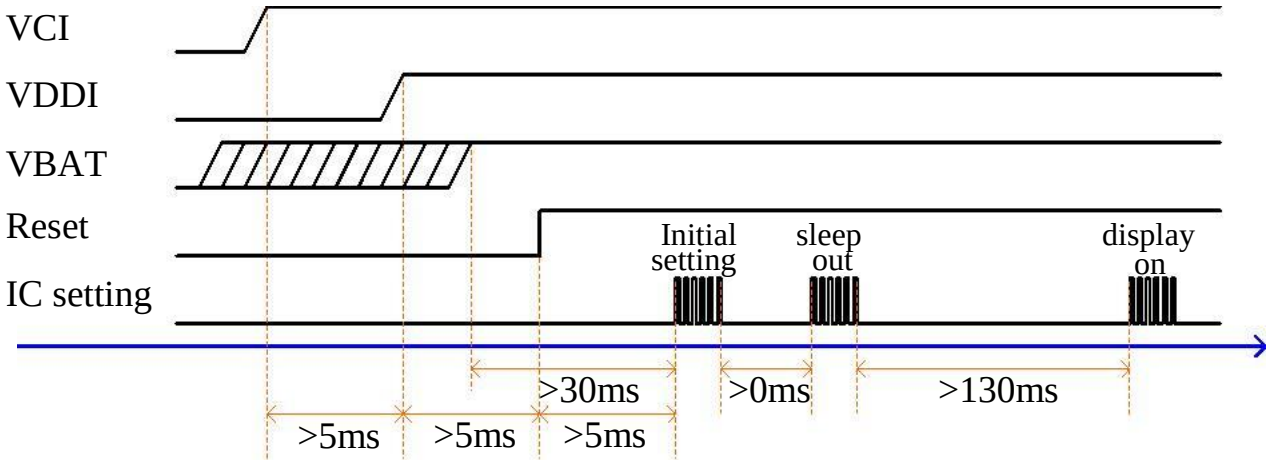
## 3. Operating Sequence

State Diagram

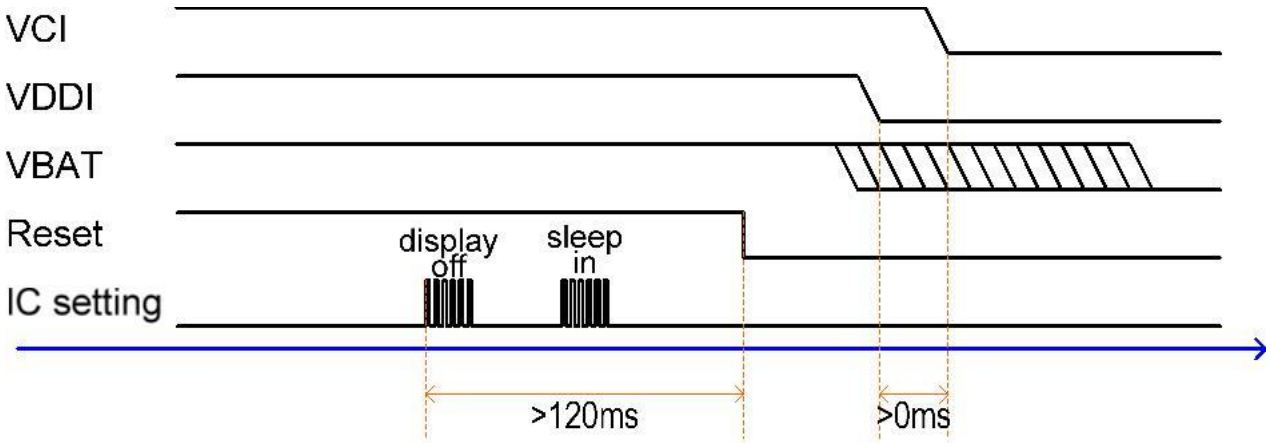



Display Power on / off Sequence

Power On Sequence:



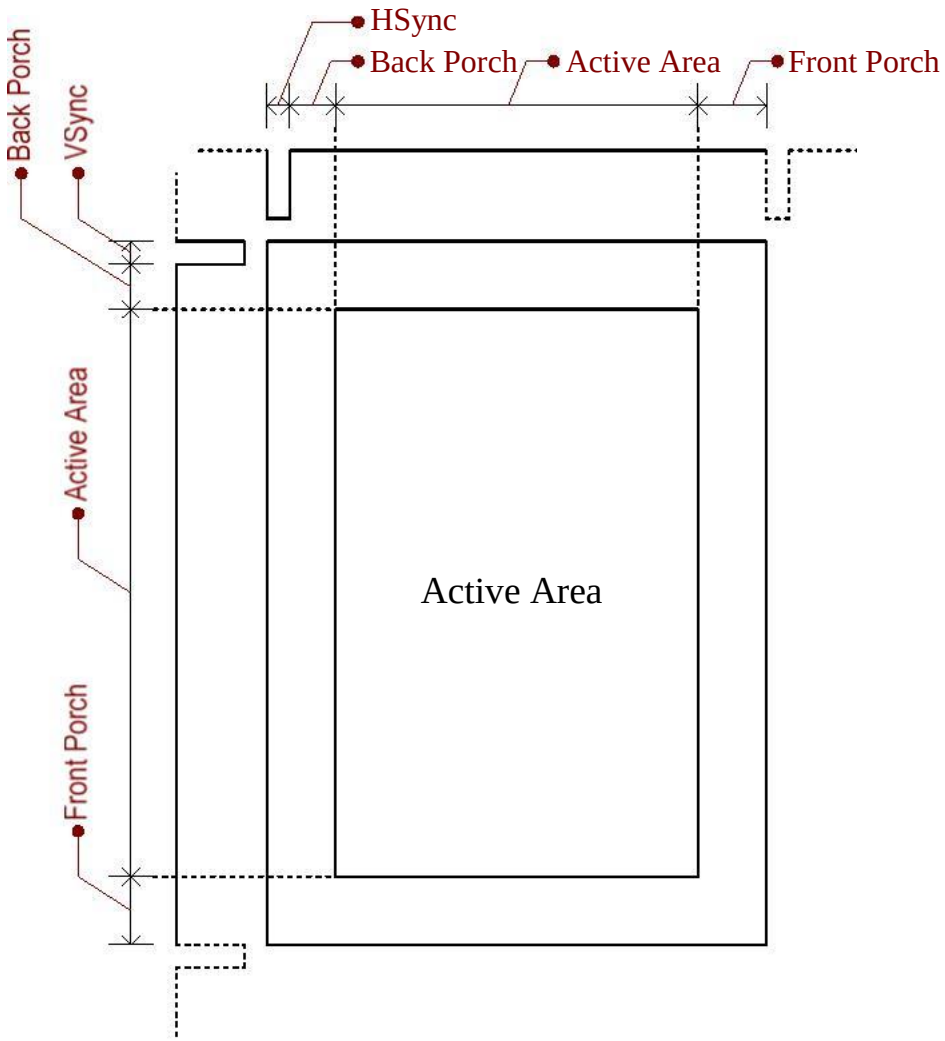
## *Power Off Sequence:*



Display Initial Setting

| Item | Parameter qt'y | address | P0 | P1 | P2 | P3 | P4 | P5 | P6 | P7 | P8 | P9 | P10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 5 | F0 | 55 | AA | 52 | 08 | 00 | | | | | | |
| 2 | 3 | B0 | 00 | 10 | 10 | | | | | | | | |
| 3 | 1 | BA | 60 | | | | | | | | | | |
| 4 | 7 | BB | 00 | 00 | 00 | 00 | 00 | 00 | 00 | | | | |
| 5 | 8 | C0 | C0 | 04 | 00 | 20 | 02 | E4 | E1 | C0 | | | |
| 6 | 8 | C1 | C0 | 04 | 00 | 20 | 04 | E4 | E1 | C0 | | | |
| 7 | 5 | F0 | 55 | AA | 52 | 08 | 02 | | | | | | |
| 8 | 1 | CA | 04 | | | | | | | | | | |
| 9 | 1 | E1 | 00 | | | | | | | | | | |
| 10 | 1 | E2 | 0A | | | | | | | | | | |
| 11 | 1 | E3 | 40 | | | | | | | | | | |
| 12 | 4 | E7 | 00 | 00 | 00 | 00 | | | | | | | |
| 13 | 8 | ED | 48 | 00 | E0 | 13 | 08 | 00 | 91 | 08 | | | |
| 14 | 6 | FD | 00 | 08 | 1C | 00 | 00 | 01 | | | | | |
| 15 | 11 | C3 | 11 | 24 | 04 | 0A | 02 | 04 | 00 | 1C | 10 | F0 | 00 |
| 16 | 5 | F0 | 55 | AA | 52 | 08 | 03 | | | | | | |
| 17 | 1 | E0 | 00 | | | | | | | | | | |
| 18 | 6 | F1 | 00 | 00 | 00 | 00 | 00 | 0B | | | | | |
| 19 | 1 | F6 | 08 | | | | | | | | | | |
| 20 | 5 | F0 | 55 | AA | 52 | 08 | 05 | | | | | | |
| 21 | 5 | C3 | 00 | 10 | 50 | 50 | 50 | | | | | | |
| 22 | 2 | C4 | 00 | 14 | | | | | | | | | |
| 23 | 1 | C9 | 04 | | | | | | | | | | |
| 24 | 5 | F0 | 55 | AA | 52 | 08 | 01 | | | | | | |
| 25 | 3 | B0 | 06 | 06 | 06 | | | | | | | | |
| 26 | 3 | B1 | 14 | 14 | 14 | | | | | | | | |
| 27 | 3 | B2 | 00 | 00 | 00 | | | | | | | | |
| 28 | 3 | B4 | 66 | 66 | 66 | | | | | | | | |
| 29 | 3 | B5 | 44 | 44 | 44 | | | | | | | | |
| 30 | 3 | B6 | 54 | 54 | 54 | | | | | | | | |
| 31 | 3 | B7 | 24 | 24 | 24 | | | | | | | | |
| 32 | 3 | B9 | 04 | 04 | 04 | | | | | | | | |
| 33 | 3 | BA | 14 | 14 | 14 | | | | | | | | |
| 34 | 3 | BE | 22 | 38 | 78 | | | | | | | | |
| 35 | 1 | 35 | 00 | | | | | | | | | | |

Display Timing




| Name | Qt'y | Unit |
|---|---|---|
| Frame Rate | 60 | Hz |
| Line Time | 12.75 | us |
| H total | 752 | dot |
| H sync | 5 | dot |
| H back porch | 11 | dot |
| H active area | 720 | dot |
| H front porch | 16 | dot |
| V total | 1312 | line |
| V sync | 5 | line |
| V back porch | 11 | line |
| V active area | 1280 | line |
| V front porch | 16 | line |

## D. Optical Specifications

| Item | | | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Brightness | | | 315 | 350 | 385 | nits | Note 3 |
| Contrast ratio | | @25deg | 10000 | -- | -- | | Note 5 |
| Viewing angle CR>1600 | | Top | 80° | -- | -- | deg | Note 7 |
| | | Bottom | 80° | -- | -- | deg | |
| | | Left | 80° | -- | -- | deg | |
| | | Right | 80° | -- | -- | deg | |
| Brightness Uniformity | | 385nits | 70% | -- | -- | | Note 6 |
| Optical Switching Time | | +25°B/W(Tr+Tf)/2 | -- | -- | 1 | ms | Note 4 |
| Color | W | CIE1931 x | 0.28 | 0.30 | 0.32 | | |
| | | CIE1931 y | 0.29 | 0.31 | 0.33 | | |
| | R | CIE1931 x | 0.645 | 0.675 | 0.705 | | |
| | | CIE1931 y | 0.295 | 0.325 | 0.355 | | |
| | G | CIE1931 x | 0.186 | 0.236 | 0.286 | | |
| | | CIE1931 y | 0.661 | 0.711 | 0.761 | | |
| | B | CIE1931 x | 0.090 | 0.130 | 0.170 | | |
| | | CIE1931 y | 0.025 | 0.065 | 0.105 | | |
| NTSC | | CIE x , y | 80 | 100 | -- | % | |
| Life time | LT95 | 25C° | 100 | -- | -- | hrs | Note 9 |
| Flicker | | | -- | -- | -30 | db | Note 8 |
| Crosstalk | | Max (H, V) | -- | -- | 6.0 | % | Note 10 |
| Gamma | | γ | 2.0 | 2.2 | 2.4 | | Note 11 |

Note 1: Ambient temperature =25℃±2℃, measured by CA-310.

Note 2: To be measured in the dark room.

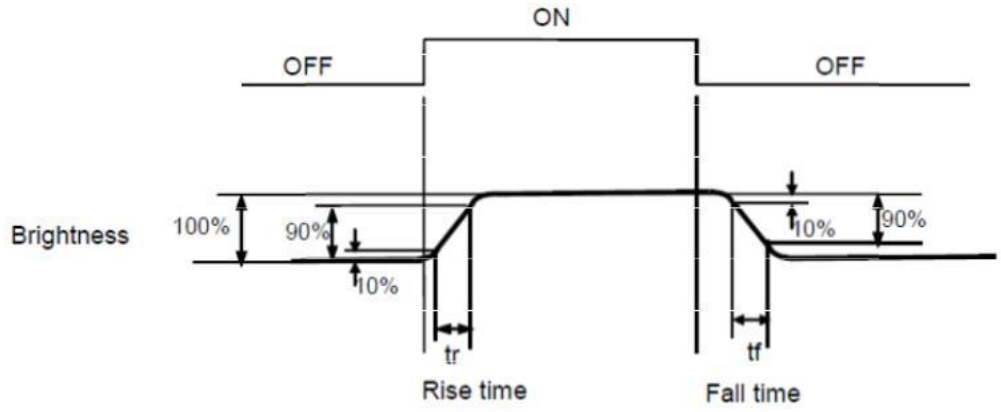
Note 3: The brightness measurement shall be done at the center of the display with a full white image.

Note 4: Optical Switching Time:

The optical switching time measurements should be performed at driven BLACK and driven WHITE at typ. brightness setting by the driving techniques specified. The luminance should be measured with the emitting display and the detector at θ=0°and ψ=90°. The rise time tr is the time between a 10% optically response of the display and a 90% optically response of the display. The fall time tf is the time



between a 10% optically response of the display and a 90% optically response to the display. The response time is defined as the average of the rise time and the fall time.

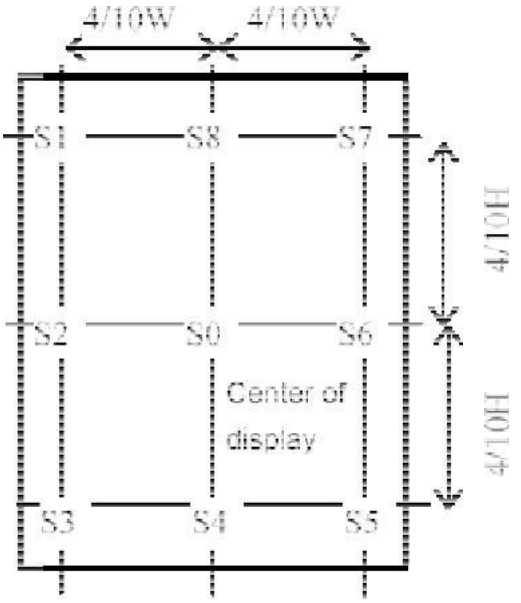



Note 5: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at "White"}}{\text{Photo detector output when OLED is at "Black}}$$

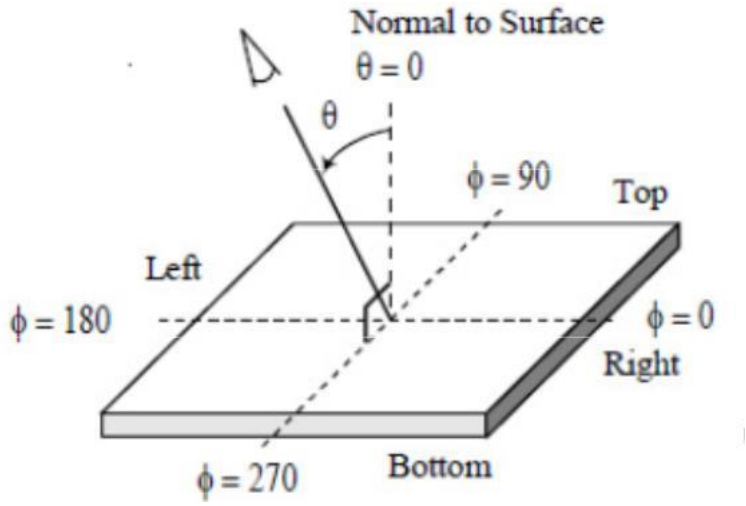
Note 6: Uniformity. Refer to figure as below




$$\text{Luminance uniformity} = \frac{\text{Minimum value from S0 to S8}}{\text{Maximum value from S0 to S8}} \times 100(\%)$$

Note 7: Definition of viewing angle :

The optical performance is specified as the driver IC located at =270°




Note 8: The panel should conform to Flicer spec. after Wahlee's FPC bonding process.

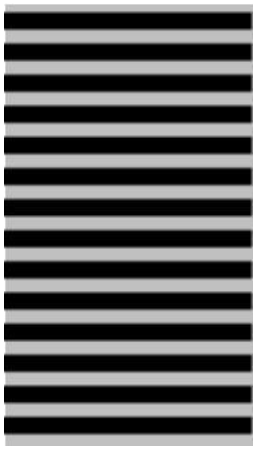
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flic\,\text{ker} = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.

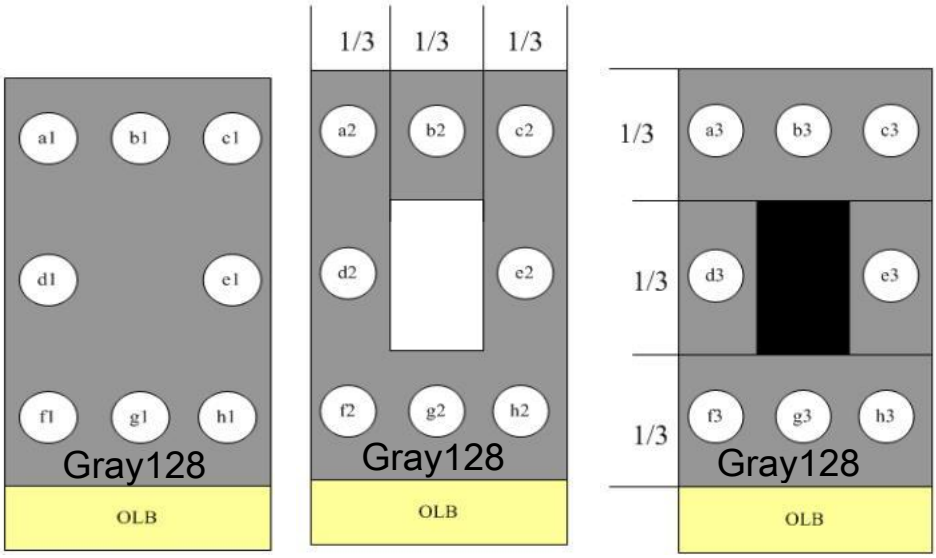


Note 9: Time to 95% Luminance

Test @ full white pattern, the brightness decay from 100% to 95%.

Note 10: Cross-talk

The panel should conform to Cross-talk spec. after Wahlee's FPC bonding process.




$$CrossTalk\_White = \begin{cases} 1-\left(\frac{b2}{a2}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b2}{c2}\div\frac{b1}{c1}\right)\times 100\% \\ 1-\left(\frac{d2}{a2}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d2}{f2}\div\frac{d1}{f1}\right)\times 100\% \\ 1-\left(\frac{e2}{c2}\div\frac{e1}{c1}\right)\times 100\%, 1-\left(\frac{e2}{h2}\div\frac{e1}{h1}\right)\times 100\% \\ 1-\left(\frac{g2}{f2}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g2}{h2}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk\_Black = \begin{cases} 1-\left(\frac{b3}{a3}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b3}{c3}\div\frac{b1}{c1}\right)\times 100\% \\ 1-\left(\frac{d3}{a3}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d3}{f3}\div\frac{d1}{f1}\right)\times 100\% \\ 1-\left(\frac{e3}{c3}\div\frac{e1}{c1}\right)\times 100\%, 1-\left(\frac{e3}{h3}\div\frac{e1}{h1}\right)\times 100\% \\ 1-\left(\frac{g3}{f3}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g3}{h3}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk = MAX\{CrossTalk\_White, CrossTalk\_Black\}$$

Note 11: Gamma spec. is based on Gray level 255, 250, 244, 240, 232, 224, 206, 192, 160, 128, 95, 63, 47 & 31.

The panel should conform to Gamma spec. after Wahlee's FPC bonding process.

## E. Reliability Test Items

| Category | No. | Test items | Conditions | Remark |
|---|---|---|---|---|
| Reliability (Environment) | 1 | High Temp. Operation | Ta= 60℃ 168hrs | Judge criteria: No function defect |
| | 2 | High Temp. Storage | Ta= 70℃ 168hrs | |
| | 3 | Low Temp. Operation | Ta= -20℃ 168hrs | |
| | 4 | Low Temp. Storage | Ta= -40℃ 168hrs | |
| | 5 | High Temp./Humi. Operation | Ta= 40℃. 90% RH 168hrs | |
| | 6 | Thermal Shock | -40℃~70℃, Dwell for 30 min. 30 cycles.<br>Non-operation | |
| | 7 | Low Pressure Storage | Condition: 40,000 ft, room temperature, 48hrs.<br>Criterion: Normal performance after recovery time. | Non-operation |
| Reliability (Mechanical) | 8 | Shock Test | Half Sine, 400G, duration time 2 ms, One shock for each surfaces,total 6 shocks | Non-operation |
| | 9 | Random Vibration Test | 0.025G2/Hz, 10~500Hz<br>Nominal 3.5Grms in each axis, 30 minutes each axis | Non-operation |
| | 10 | Sinusoidal Vibration Test | 0.5 octave / minutes sweep rate<br>One sweep, 10 to 500Hz, all 3 axes (X, Y, Z)<br>Fixture used: Fasten the specimen to the vibration table<br>Power is OFF | Non-operation |

# F. Precaution

Please pay attention to the following items when you use OLED Modules/Panels:

1. Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).
5. Less EMI: it will be more safety and less noise.
6. Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Please be sure to turn-off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).
15. Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.
16. Please avoid any static electricity damage (ESD) during producing and operating.
17. Do not disassemble and reassemble the module(panel) by self.
18. Be careful do not touch the rear side directly.
19. No strong vibration or shock. It will cause module(panel) broken.
20. Storage the modules(panel) in suitable environment with regular packing.
21. Be careful of injury from a broken display module(panel).
22. Please avoid the pressure adding to the surface (front or rear side) of modules(panel), because it will cause the display non-uniformity or other function issue.
23. The temperature of FOG process ( bonding process of FPC ) maybe effect the COG status. Please optimize the patameter of FOG process.
24. The ACF of FOG must be selected carefully to avoid any failure or damage for panel.
25. The touch IC must be followed the suggestion from Wahlee for the best performance of touch function.
26. To get better optical performance and reduce the accumulation of static electricity, we suggest to add shelter tape which contains metal foil on the back-side of panel.

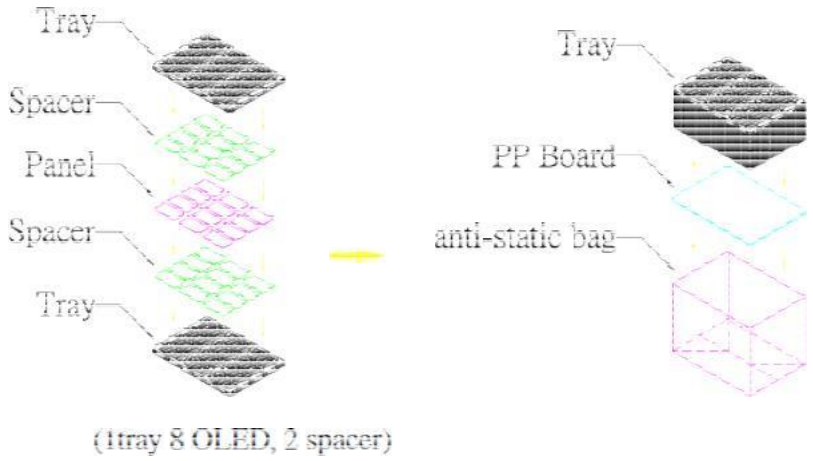


# G. Packing

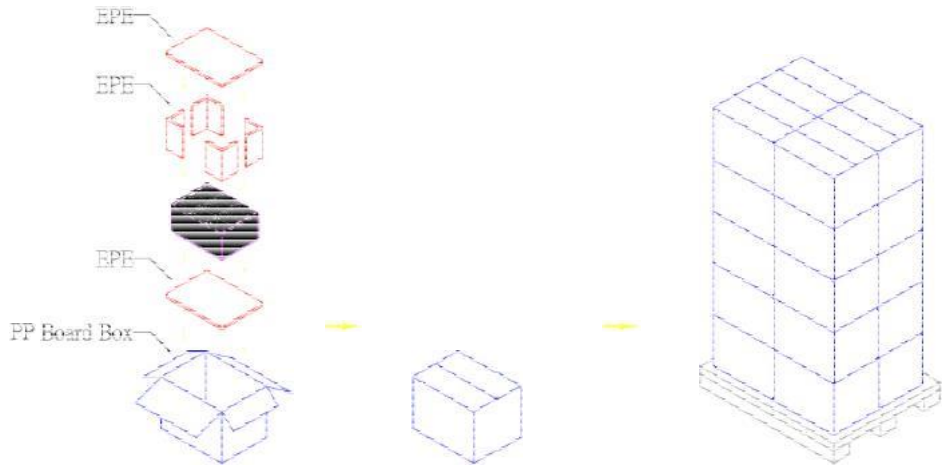
紙箱尺寸:546mm x 406mm x 278mm

棧板尺寸:1150mmx840mmx132mm

1set for 20 tray (8pcs) +1 tray(空) =160pcs module




(1tray 8 OLED, 2 spacer)




5 layer x4 boxes
=20 boxes

# H. Outline Demension (Cell Glass + Driver IC + POL)