5.46 inch AMOLED
SPECIFICATION
MODEL NAME: LETB2055ZMN1

Date: 2016 / 05 / 24

Customer Signature		
Customer		
Approved Date	**Approved By**	**Reviewed By**

Record of Revision

Version	Revise Date	Page	Content
1.0	2016/01/07	1~32	First Draf t
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3.0	2016/05/24	4 23	Phys ical Spec if ications Outline Dimens ion

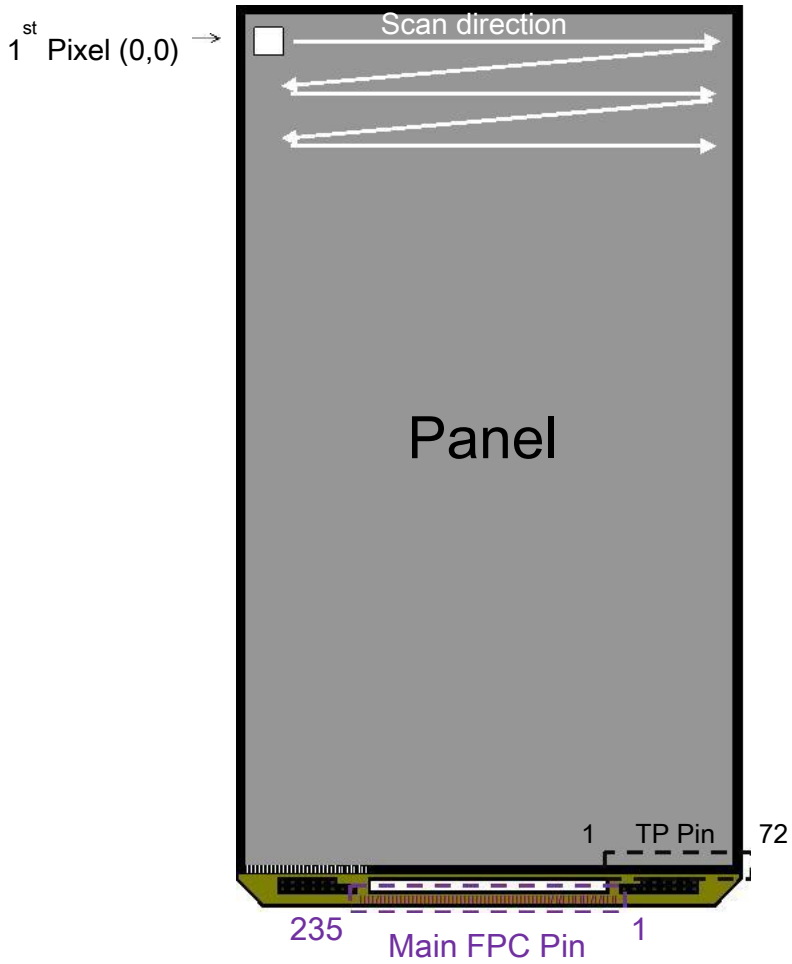
Contents

A. General Specification

1. Physical Specifications

NO	Item	unit	Specification	Remark
1	Screen Size	inch	5.46”	Diagonal
2	Display Resolution	--	1080(H) X 1920(V)	Full HD
3	Outline Dimension	mm	70.84 (H) × 128.01(V) × 0.759(T)	
4	Active Area	mm	68.04 (H)×120.96(V)	
5	Pixel Pitch	um	63	
6	Color Configuration	--	R, G, B	
7	Color Depth	--	16.7M	8-bit x RGB
8	NTSC Ratio	%	100	CIE1931
9	Display Mode	--	AMOLED	
10	Panel Surface Treatment	--	Hard Coat (3H)	
11	Interface	--	MIPI DSI – Video Mode	
12	Driver IC		RM69071	
13	Touch IC		S3508	
14	Multi-finger Touch		10	

2. Mechanical Schematic



3. Main FPC Pin Assignment

#	Pin_name	I/O/P	Description	Note
1	DUMMY_1	-	Open	
2	OVSS_01	P	OLED Power	
3	OVSS_02	P		
4	OVSS_03	P		
5	OVSS_04	P		
6	OVSS_05	P		
7	OVSS_06	P		
8	OVSS_07	P		
9	OVSS_08	P		
10	OVSS_09	P		
11	OVSS_10	P		
12	DUMMY_02	-	Open	
13	OVDD_00	P		
14	OVDD_01	P		
15	OVDD_02	P		
16	OVDD_03	P		
17	OVDD_04	P		
18	OVDD_05	P		
19	OVDD_06	P		
20	OVDD_07	P		
21	OVDD_08	P		
22	OVDD_09	P	OLED Power	
23	OVDD_10	P		
24	OVDD_11	P		
25	OVDD_12	P		
26	OVDD_13	P		
27	OVDD_14	P		
28	OVDD_15	P		
29	OVDD_16	P		
30	OVDD_17	P		
31	OVDD_18	P		
32	OVDD_19	P		
33	DUMMY_03	-	Open	
34	MTP_PWR	O	Open	Note1
35	VDDB_01	P	Driver IC Analog Power Supply	Note5
36	VDDB_02	P		
37	VDDB_03	P	Driver IC Analog Power Supply	Note5

38	VSSR_01	P	GND	
39	VREFP_01	O	IC Internal Regulator Output	
40	VREFN_01	O	NC	
41	VGLR_01	O	Driver IC Regulator Output	
42	VGLR_02	O		
43	VGHR_01	O	Driver IC Regulator Output	
44	VGHR_02	O		
45	AVDD_01	P	Driver IC Source Analog Power	
46	AVDD_02	P		
47	AVDD_03	P		
48	AVDD_04	P		
49	VSSB_01	P	GND	
50	C51P_01	I/O	Charge Pump Capacitor	
51	C51P_02	I/O		
52	C51N_01	I/O	Charge Pump Capacitor	
53	C51N_02	I/O		
54	VSSB_02	P	GND	
55	VSSB_03	P	GND	
56	C52P_01	I/O	Charge Pump Capacitor	
57	C52P_02	I/O		
58	C52N_01	I/O	Charge Pump Capacitor	
59	C52N_02	I/O		
60	AVEE_01	O	Driver IC Regulator Output	
61	AVEE_02	O		
62	AVSS_01	P	GND	
63	VCC_01	P	Driver IC Digital Power Supply	
64	VCC_02	P		
65	VCC_03	P		
66	VCC_04	P		
67	DVDD_01	O	Driver IC Regulator Output	
68	DVDD_02	O		
69	DVSS_01	P	GND	
70	REXS_01	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.	
71	REXS_02	I		
72	TE1_01	O	Open	
73	TE1_02	O		

74 75	TE_01 TE_02	O O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/Wcommand. When this pin is not activated, this pin is output low. If not used, please open this pin.	
76 77	OLED_EN_01 OLED_EN_02	O O	DC/DC power IC control signal. Connect to power IC EN pin	
78	SWIRE_01	O	DC/DC power IC control signal Connect to power IC CTRL pin	
79	SDO	O	Open	Note2
80	SDI	I/O	GND	Note3
81	SCL	I	GND	
82	CSX	I	GND	
83	DCX	I	GND	
84	DSWAP[2]	I	Driver IC Digital Power Supply	Note4 Note5
85	DSWAP[1]	I	Driver IC Digital Power Supply	
86	DSWAP[0]	I	GND	
87	PSWAP	I	Driver IC Digital Power Supply	
88	VSSI_01	P	GND	
89	VDDI_01	P	Driver IC Digital Power Supply	Note5
90	VDDI_02	P		
91	VDDI_03	P		
92	VDDI_04	P		
93	VDDI_05	P		
94	VDDI_06	P		
95	VDDI_07	P		
96	VDDI_08	P		
97	VDDI_09	P		
98	VDDI_10	P		
99	VDDI_11	P		
100	VSSAM_01	P	GND	
101	HSSI_D0_N	I/O	MIPI DSI Data2+	Note4
102	HSSI_D0_P	I/O	MIPI DSI Data2-	
103	VSSAM_02	P	GND	
104	HSSI_D1_N	I/O	MIPI DSI Data1+	Note4
105	HSSI_D1_P	I/O	MIPI DSI Data1-	
106	DUMMY_04	-	GND	
107	VSSAM_03	P	GND	
108	HSSI_CLK_N	I	MIPI DSI Clock+	Note4
109	HSSI_CLK_P	I	MIPI DSI Clock-	

110	VSSAM_04	P	GND	
111	HSSI_D2_N	I/O	MIPI DSI Data0+	Note4
112	HSSI_D2_P	I/O	MIPI DSI Data0-	
113	DUMMY_05	-	GND	
114	VSSAM_05	P	GND	
115	HSSI_D3_N	I/O	MIPI DSI Data3+	Note4
116	HSSI_D3_P	I/O	MIPI DSI Data3-	
117	VSSAM_06	P	GND	
118	MVDDA_01	O	Driver IC Regulator Output	
119	MVDDA_02	O		
120	MVDDA_03	O		
121	MVDDA_04	O		
122	MVDDA_05	O		
123	MVDDA_06	O		
124	MVDDA_07	O		
125	MVDDA_08	O		
126	MVDDA_09	O		
127	VDDAM_01	P	Driver IC Digital Power Supply	Note5
128	VDDAM_02	P		
129	VDDAM_03	P		
130	VCC_05	P	Driver IC Digital Power Supply	Note5
131	VCC_06	P		
132	DVDD_03	O	Driver IC Regulator Output	
133	DVDD_04	O		
134	DVSS_02	P	GND	
135	DVSS_03	P		
136	VDDR_01	P	Driver IC Analog Power Supply	Note5
137	VDDR_02	P		
138	VDDA_01	P	Driver IC Analog Power Supply	Note5
139	VDDA_02	P		
140	VSSA_01	P	GND	
141	AVSS_02	P	GND	
142	VGMP	O	Driver IC Regulator Output	
143	VGSP	O	Driver IC Regulator Output	
144	VREF	O	Driver IC Regulator Output	
145	VSSB_04	P	GND	
146	VDDB_04	P	Driver IC Analog Power Supply	Note5
147	VDDB_05	P	Driver IC Analog Power Supply	
148	VCL_01	O	Driver IC Regulator Output	

149	VCL_02	O	Driver IC Regulator Output	
150	C41P_01	I/O	Charge Pump Capacitor	
151	C41P_02	I/O	Charge Pump Capacitor	
152	C41N_01	I/O	Charge Pump Capacitor	
153	C41N_02	I/O	Charge Pump Capacitor	
154	C42P_01	I/O	Charge Pump Capacitor	
155	C42P_02	I/O	Charge Pump Capacitor	
156	C42N_01	I/O	Charge Pump Capacitor	
157	C42N_02	I/O	Charge Pump Capacitor	
158	AVDD_05	P	Driver IC Source Analog Power	
159	AVDD_06	P		
160	AVDD_07	P		
161	AVDD_08	P		
162	AVEE_03	O	Driver IC Regulator Output	
163	AVEE_04	O		
164	C21P_01	I/O	Charge Pump Capacitor	
165	C21P_02	I/O	Charge Pump Capacitor	
166	C21N_01	I/O	Charge Pump Capacitor	
167	C21N_02	I/O	Charge Pump Capacitor	
168	C22P_01	I/O	Charge Pump Capacitor	
169	C22P_02	I/O	Charge Pump Capacitor	
170	C22N_01	I/O	Charge Pump Capacitor	
171	C22N_02	I/O	Charge Pump Capacitor	
172	VGH	O	Driver IC Regulator Output	
173	VDDB_06	P	Driver IC Analog Power Supply	Note5
174	VDDB_07	P		
175	VSSB_05	P	GND	
176	C23P_01	I/O	Charge Pump Capacitor	
177	C23P_02	I/O	Charge Pump Capacitor	
178	C23N_01	I/O	Charge Pump Capacitor	
179	C23N_02	I/O	Charge Pump Capacitor	
180	C24P_01	I/O	Charge Pump Capacitor	
181	C24P_02	I/O	Charge Pump Capacitor	
182	C24N_01	I/O	Charge Pump Capacitor	
183	C24N_02	I/O	Charge Pump Capacitor	
184	VGL_01	O	Driver IC Regulator Output	
185	VGL_02	O		
186	DVDD_05	O	Driver IC Regulator Output	
187	DVDD_06	O		

188	DVSS_04	P	GND	
189	DVSS_05	P		
190	VGHR_03	O	Driver IC Regulator Output	
191	VGHR_04	O		
192	VGLR_03	O	Driver IC Regulator Output	
193	VGLR_04	O		
194	VSSR_02	P	GND	
195	VSSR_03	P		
196	VDDR_03	P	Driver IC Analog Power Supply	Note5
197	VDDR_04	P		
198	VDDR_05	P		
199	VREFN_02	O	Open	
200	VREFP_02	O	Driver IC Regulator Output	
201	DUMMY_06	-	Open	
202	DUMMY_07	-	Open	
203	DUMMY_08	-	Open	
204	OVDD_20	P	OLED Power	
205	OVDD_21	P		
206	OVDD_22	P		
207	OVDD_23	P		
208	OVDD_24	P		
209	OVDD_25	P		
210	OVDD_26	P		
211	OVDD_27	P		
212	OVDD_28	P		
213	OVDD_29	P		
214	OVDD_30	P		
215	OVDD_31	P		
216	OVDD_32	P		
217	OVDD_33	P		
218	OVDD_34	P		
219	OVDD_35	P		
220	OVDD_36	P		
221	OVDD_37	P		
222	OVDD_38	P		
223	OVDD_39	P		
224	DUMMY_09	-	Open	
225	OVSS_11	P	OLED Power	
226	OVSS_12	P		

227	OVSS_13	P	OLED Power	
228	OVSS_14	P		
229	OVSS_15	P		
230	OVSS_16	P		
231	OVSS_17	P		
232	OVSS_18	P		
233	OVSS_19	P		
234	OVSS_20	P		
235	DUMMY_10	-	Open	

Note1: Not accessible for user, this pin must be open.

Note2: When using MIPI I/F, this pin must be open.

Note3: When using MIPI I/F, this pin must be connected to GND.

Note4: This pin is for MIPI I/F. Please reference driver IC datasheet for using instruction. If this pin not used, must be connected to GND.

Note5: VDD (Driver IC Analog Power Supply) is provided by VCI, and VDDI (Driver IC Digital Power Supply) is provided by IOVCC.

4. TP Pin Assignment

FPC Pin No	Symbol
1	Dummy
2	Open
3	Open
4	GND
5	GUARD0_Y
6	Y15
7	Y14
8	Y13
9	Y12
10	Y11
11	Y10
12	Y9
13	Y8
14	Y7
15	Y6
16	Y5
17	Y4
18	Y3
19	Y2
20	Y1
21	Y0
22	GUARD1_Y
23	Y0
24	Y1

FPC Pin No	Symbol
25	Y2
26	Y3
27	Y4
28	Y5
29	Y6
30	Y7
31	Y8
32	Y9
33	Y10
34	Y11
35	Y12
36	Y13
37	Y14
38	Y15
39	GUARD2_Y
40	X27
41	X26
42	X25
43	X24
44	X23
45	X22
46	X21
47	X20
48	X19

FPC Pin No	Symbol
49	X18
50	X17
51	X16
52	X15
53	X14
54	X13
55	X12
56	X11
57	X10
58	X9
59	X8
60	X7
61	X6
62	X5
63	X4
64	X3
65	X2
66	X1
67	X0
68	GUARD3_Y
69	GND
70	Open
71	Open
72	Dummy

Note: “X” is “Rx,” “Y” is “Tx.”

“Dummy” must be open.

“GUARD0_Y,” “GUARD1_Y ,” “GUARD2_Y,” “GUARD3_Y,” is “Guard Ring Pin.”

5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
OLED Power supply	OVDD	-	4.6	V	
OLED Power supply	OVSS	-	-2.9	V	
Driver IC Source output power supply	AVDD	-	5.8	V	
Digital Power supply	IOVCC	-0.3	+1.95	V	
Analog Power supply	VCI	-0.3	+3.2	V	
Touch analog power supply	TP_VCC	-0.3	+4.0	V	
Touch digital power supply	TP_VDDI	-0.3	+2.0	V	

Note: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

B. DC Characteristics

1. Typical Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
OLED Power supply		OVDD	-	4.6	-	V	
OLED Power supply		OVSS	-	-2.9	-	V	
Driver IC Source output power supply		AVDD	-	5.8	-	V	
Digital Power supply		IOVCC	1.65	1.8	1.95	V	
Analog Power supply		VCI	2.8	3.1	3.2	V	
Touch analog power supply		TP_VCC	2.7	3.1	3.6	V	
Touch digital power supply		TP_VDDI	1.65	1.8	1.95	V	
Input Signal Voltage	H Level	V_{IH}	0.8* IOVCC	-	IOVCC	V	RESX
	L Level	V_{IL}	0	-	0.2* IOVCC	V	
Output Signal Voltage	H Level	V_{OH}	0.8* IOVCC	-	IOVCC	V	TE
	L Level	V_{OL}	0	-	0.2* IOVCC	V	

Note1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note2:

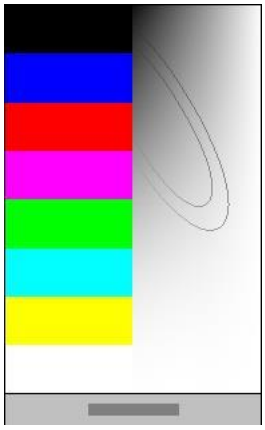
Name	P/N	Vender	Note
Power IC	TPS65632RTER	TI	Not TPS65632A (can't be used)
	RT4720A	Richtek	
TP IC	S3508	Synaptics	

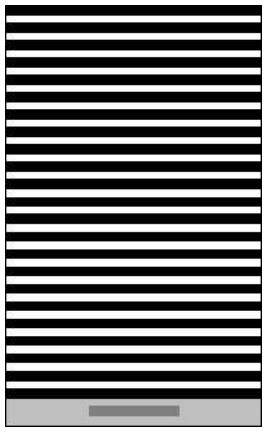
Wahlee don't suggest use other IC instead of above IC, since they are not qualified by Wahlee.

2. Display Current Consumption

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Normal	IAVDD	AVDD = 5.8V VCI = 3.1V IOVCC = 1.8V OVDD = 4.6V OVSS = -2.9V 25℃	-	15	30	mA	Note 1
	IVCI		-	3	3	mA	
	IIOVCC		-	38	40	mA	
	IOVDD		-	190	200	mA	Note 2
	IOVSS		-	190	200	mA	
DSTB (Deep Standby Mode)	IAVDD		-	0.2	1	uA	
	IVCI		-	2	3	mA	
	IIOVCC		-	25	30	uA	
	IOVDD		-	0	0	uA	
	IOVSS		-	0	0	uA	

Note 1: Typ. Test Pattern Max. Test Pattern





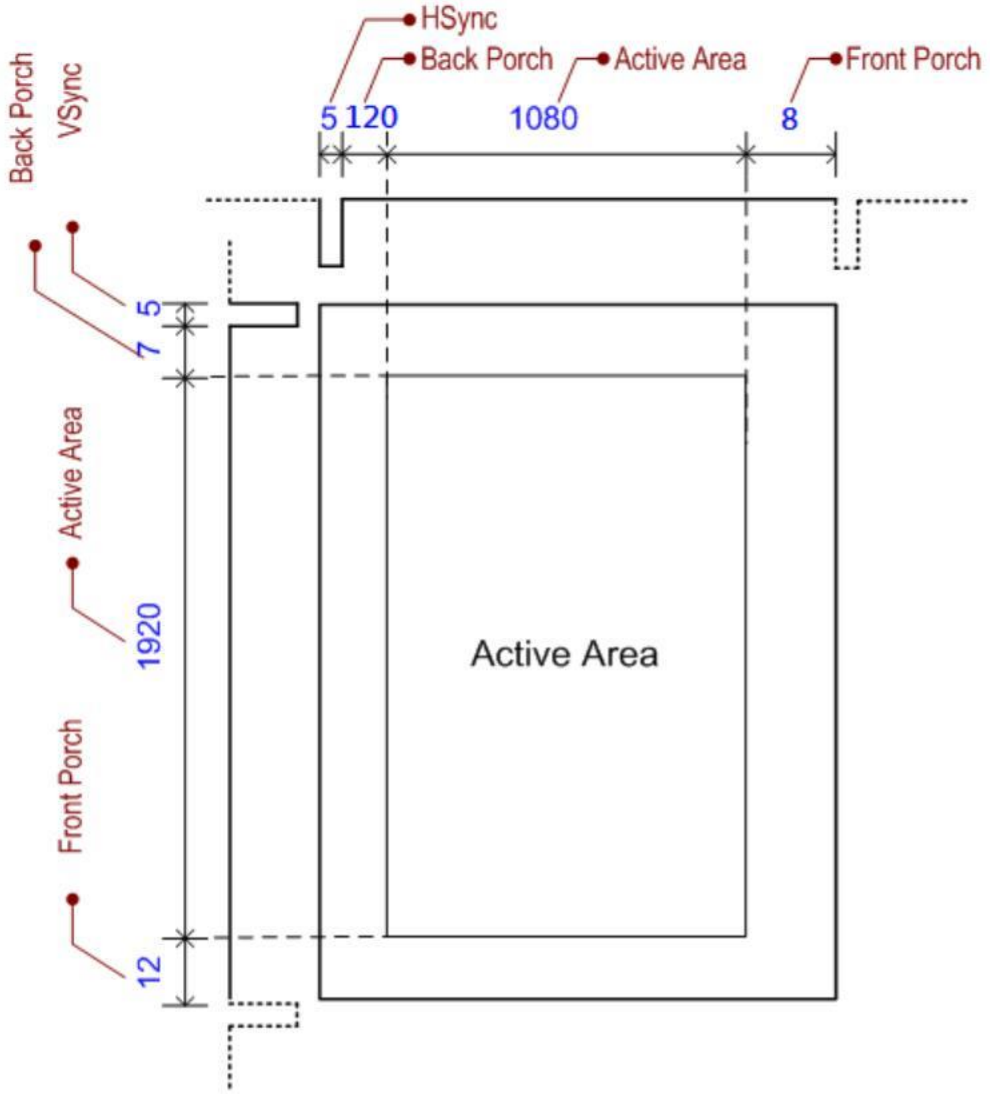
Note 2: Test pattern is “350 nits White pattern.”

3. Touch Panel Current Consumption

Mode	Symbol	Condition	Min	Typ.	Max	Unit
Active (1finger)	I_{TP_VDDI}	TP_VDDI = 1.8V TP_VCC=3.1V Report Rate: 100Hz Doze Interval: 30 ms (28Rx, 16Tx)	-	18	20	mA
	I_{TP_VCC}		-	12	14	mA
Active (10fingers)	I_{TP_VDDI}		-	25	28	mA
	I_{TP_VCC}		-	12	14	mA
Normal Operation	I_{TP_VDDI}		-	0.4	0.5	mA
	I_{TP_VCC}		-	0.4	0.5	mA
Sensor Sleep (Deep sleep)	I_{TP_VDDI}		-	7	8	μA
	I_{TP_VCC}		-	6	7	μA

C. AC Characteristics

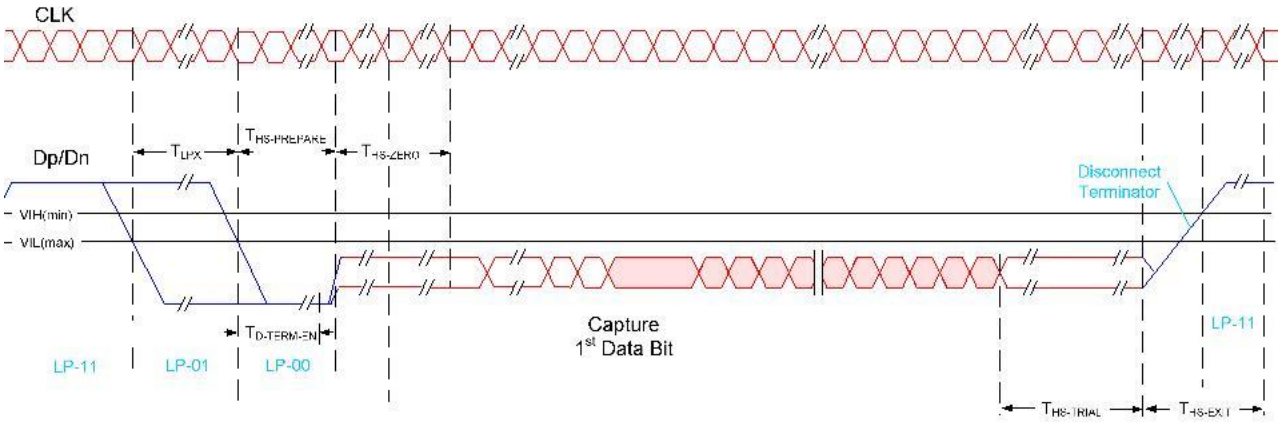
1. Display Video Timing



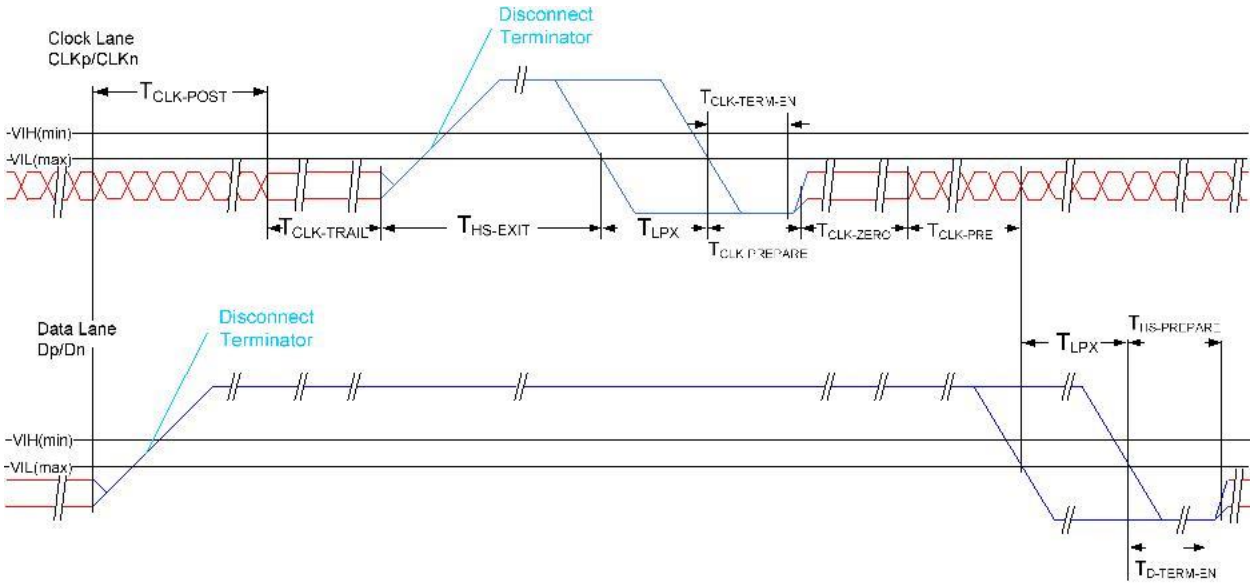
Name	Qt'y	Unit
Frame Rate	60	Hz
Line Time	8.57	us
H total	1213	Dot
H sync	5	Dot
H back porch	120	Dot
H active area	1080	Dot
H front porch	8	Dot
V total	1944	Line
V sync	5	Line
V back porch	7	Line
V active area	1920	Line
V front porch	12	Line

2. MIPI Interface Characteristics

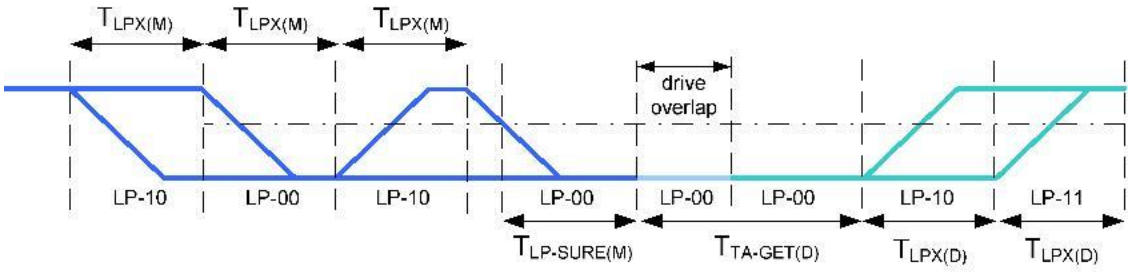
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure



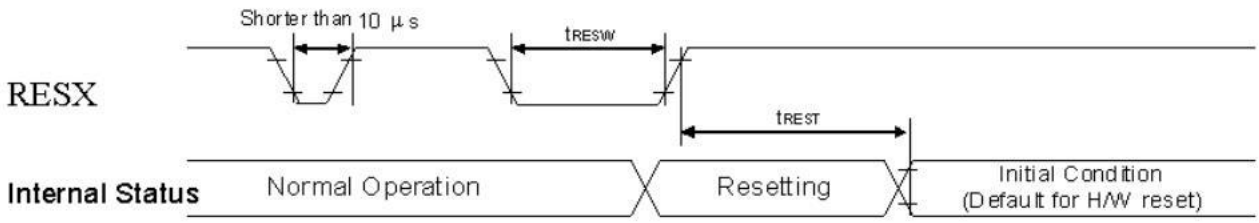
Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38 95	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38			ns UI
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI 50			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module			150	ns

$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

3. Display RESET Timing Characteristics

Reset input timing



IOVCC=1.65 to 1.95V, VCI=2.8 to 3.2V, GND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	µs
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

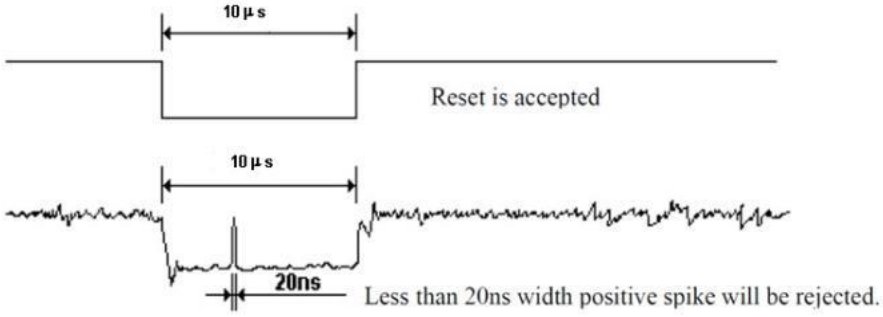
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialization Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

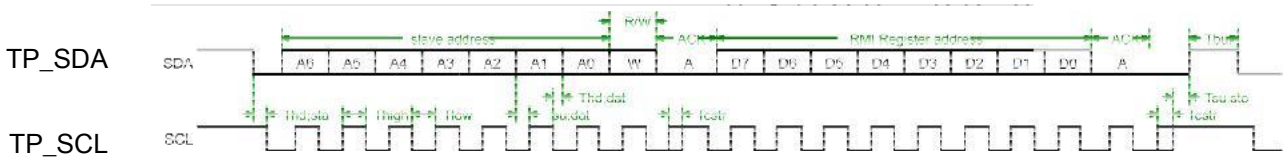


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Touch Panel I2C Timing Characteristics

I2C address: 0x20

I2C timing

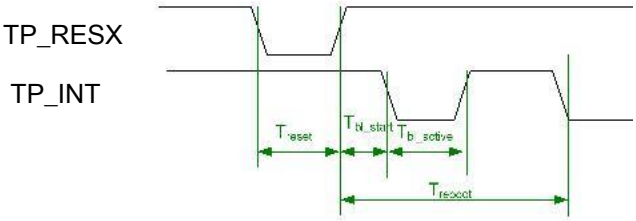


Timing Parameters

Symbol	Parameter	Standard- Mode Host		Fast-Mode Host		Unit
		Min.	Max.	Min.	Max.	
fSCL	TP_SCL clock frequency	-	100	-	400	kHz
Tcstr	Stretch time	-	25	-	25	µs
Thd;sta	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	-	0.6	-	µs
Tlow	LOW period of the TP_SCL clock	4.7	-	1.3	-	µs
Thigh	HIGH period of the TP_SCL clock	4.0	-	0.6	-	µs
Tsu;sta	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
Thd;dat	Data hold time	0	3.45	0	0.9	µs
Thd;dato	Data out hold time	-	0	-	0	µs
Tsu;dat	Data set-up time	250	-	100	-	ns
Tr	Rise time of both TP_SDA and TP_SCL signals	-	1000	20 + 0.1 Cb	300	ns
Tf	Fall time of both TP_SDA and TP_SCL signals	-	300	20 + 0.1 Cb	300	ns
Tsu:sto	Set-up time for STOP condition	4.0	-	0.6	-	µs
tBUF	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
Cb	Capacitive load for each bus line	-	400	-	400	pF
VnL	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 TP_VDDI		0.1 TP_VDDI		V
VnH	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 TP_VDDI	-	0.2 TP_VDDI	-	V

5. Touch Panel RESET Timing Characteristics

Reset input timing

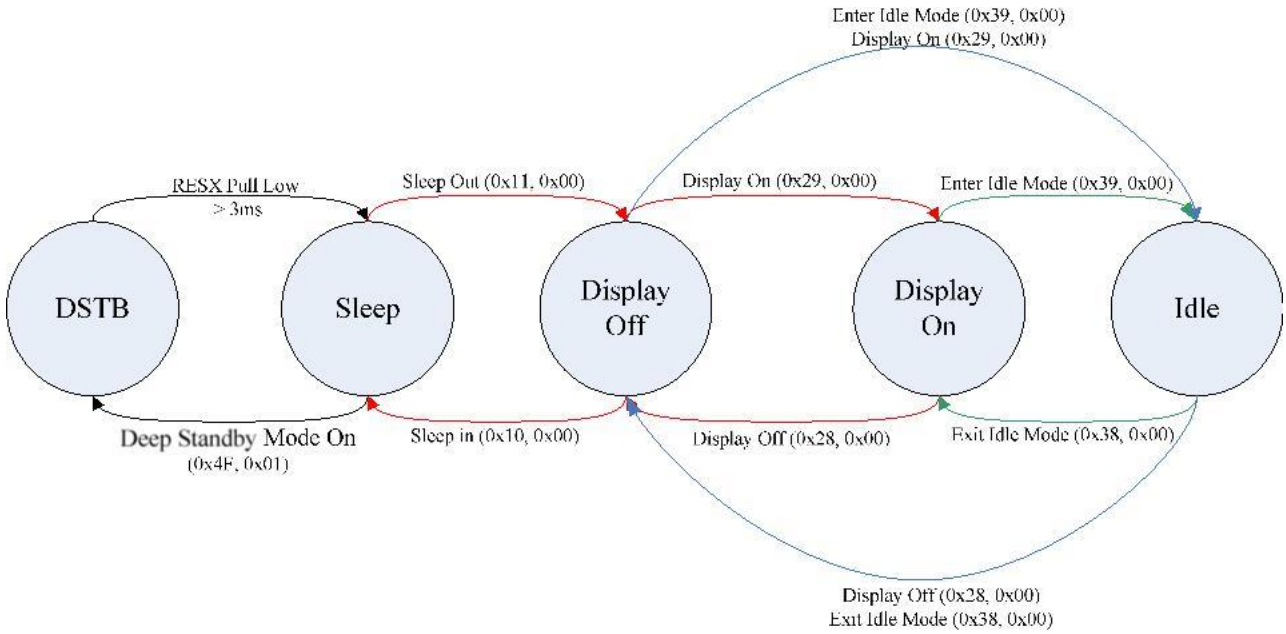


Timing Parameters

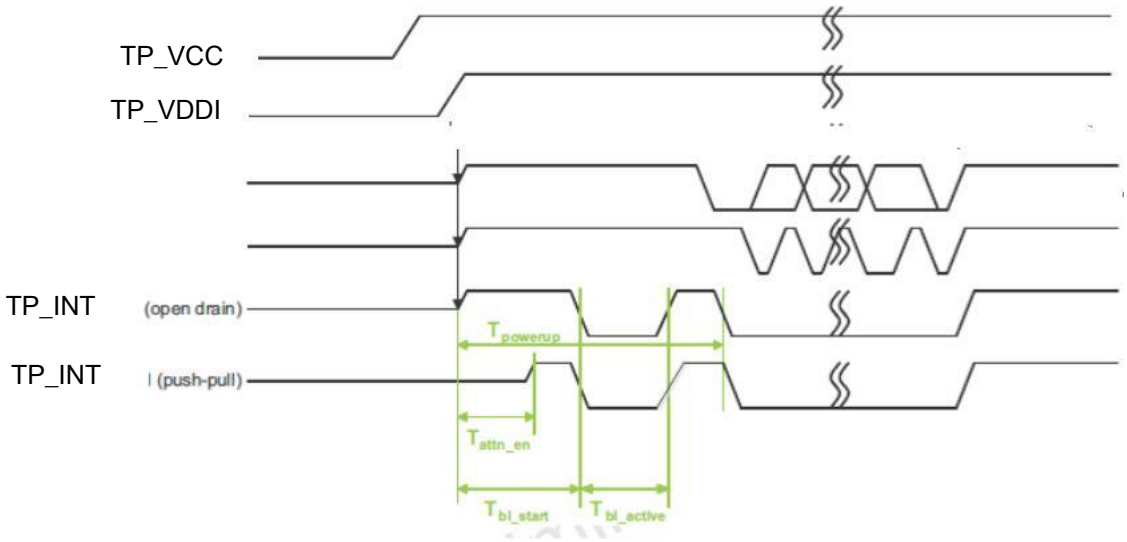
Symbol	Min.	Max.	Unit
T_{reset} (TP_RESX)	100	-	ns
T_{bl_start}	-	2	ms
T_{bl_active}	-	11	ms
T_{reboot}	-	16	ms

6. Recommended Operating Sequence

State Diagram



Touch Panel Power on Sequence



Symbol	Min.	Max.	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	-	60	ms
T_{bl_start} (bootloader start)	-	46	ms
T_{bl_active} (bootloader active)	-	11	ms

D. Optical Specification

All optical specifications are measured under typical condition. (Note 1)

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Brightness		Y @ θ=0°	280	350		nits	Note 2
Contrast ratio		@ θ=0°	10000	--	--	--	
		@ θ=60o	3000	--	--	--	
		@ θ=80o	1600	--	--	--	
Viewing angle (CR > 1600)		Top	80	--	--	Deg.	
		Bottom	80	--	--	Deg.	
		Left	80	--	--	Deg.	
		Right	80	--	--	Deg.	
Chromacity (CIE1931)	Red	x	0.640	0.670	0.700	--	Note 3
		y	0.300	0.330	0.360	--	
	Green	x	0.186	0.236	0.286	--	
		y	0.661	0.711	0.761	--	
	Blue	x	0.090	0.130	0.170	--	
		y	0.025	0.065	0.105	--	
	White	x	0.28	0.30	0.32	--	
		y	0.29	0.31	0.33	--	
Uniformity		9 points	70	80	--	%	Note 4
Flicker			--	--	-30	db	Note 5
Crosstalk			--	--	4.0	%	Note 6
Life Time		95% @ 25°C	100			hrs	Note 7

Please follow Wahlee's main FPC design suggestion.

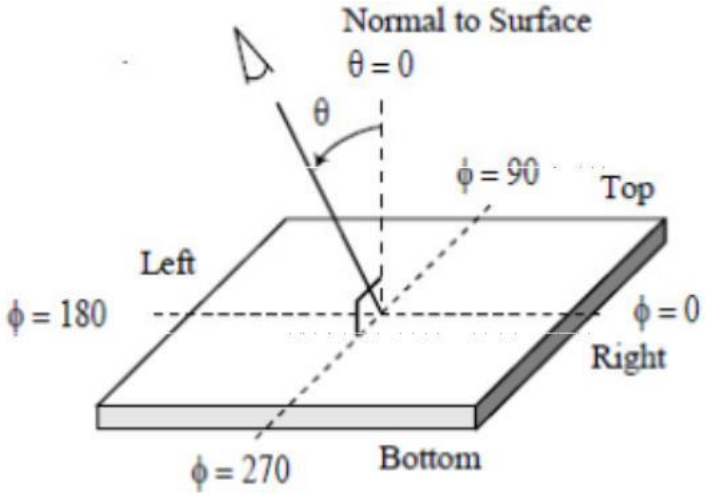
If you don't follow the Wahlee's main FPC design suggestion, then optical performance is not guaranteed.

Note 1: Typical Condition

Optical characteristics should be measured at the center area of the display with Konica Minolta CA-310 and at the ambient temperature = 25 ℃±2 ℃and in the dark room.

Note 2: Viewing Angle & Contrast Ratio

The optical performance is specified as the driver IC located at ϕ=270°.



Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White”}}{\text{Photo detector output when OLED is at “Black” pattern}}$$

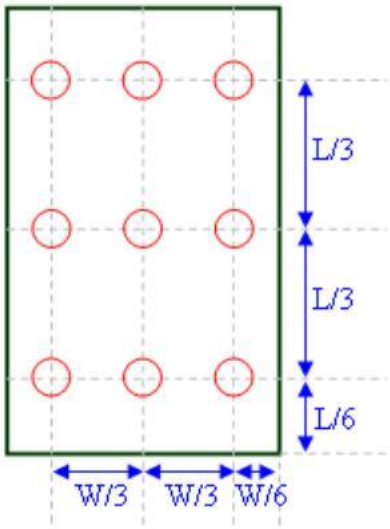
Note 3: Chromacity

Chromacity of R, G, B pattern are measured at Gray Level “255”.

Chromacity of White pattern are measured at Gray Level “255”.

Note 4: Uniformity

Uniformity under White(L255) pattern = $\frac{\text{minimum luminance of 9}}{\text{maximum luminance of 9 points}}$



Note 5: Flicker

Suggested Instruments: Konica Minolta CA-310

Measuring Point: Center point of 128th gray

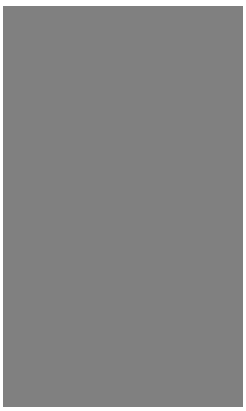
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad (dB)$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

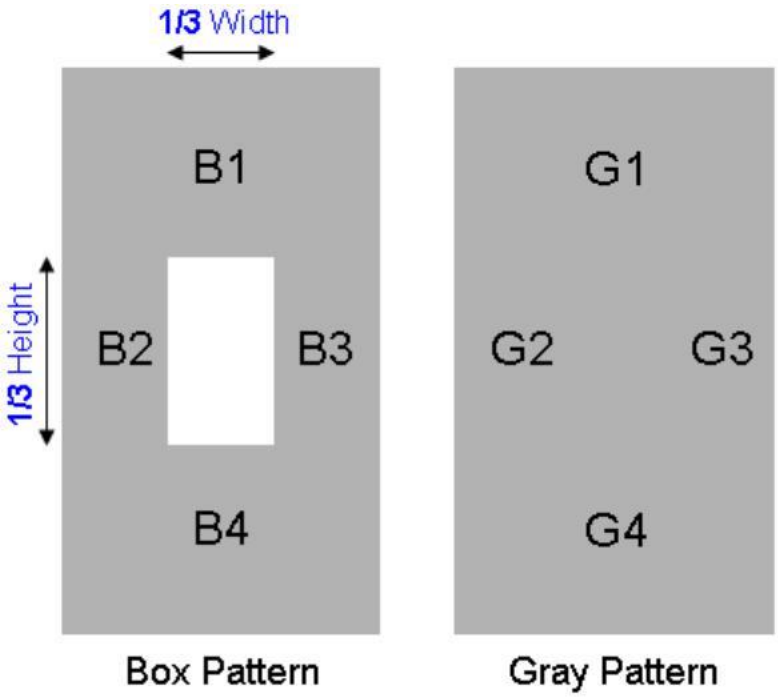
Test Pattern: L128 Gray



Note 6: Crosstalk

Crosstalk shall be calculated by the luminance of B1~B4 and G1~G4 in the patterns shown below.

Box Pattern: L128 gray level background with a L255 White window in the central area.
Gray Pattern: L128 gray level background only.



$$\text{Crosstalk} \equiv \text{Maximum} : \left| \frac{B1-G1}{G1}, \frac{B2-G2}{G2}, \frac{B3-G3}{G3}, \frac{B4-G4}{G4} \right| \times 100\%$$

Note 7: Life Time

OLED life time is defined by the Minimum Duration Time that the luminance is decayed to a specific ratio (ex. 95%) of initial state.

Test Pattern under duration period: L255 White

E. Reliability Test Items

In the standard condition, there should not be any display function NG issue occurred during the reliability test and the performance is confirmed after panel is left at room temperature.
All the cosmetic specifications are judged only before the reliability stress.

No.	Test items	Conditions		Remark
1	High Temperature Storage	T= 80℃	100Hrs	Note 1
2	Low Temperature Storage	T= -30℃	100Hrs	
3	High Temperature Operation	T= 70℃	100Hrs	
4	Low Temperature Operation	T= -20℃	100Hrs	
5	High Temperature & Humidity Operation	T= 60℃. 90% RH	100Hrs	
6	Thermal Shock	-30℃ ~ 80℃, 30 cycle, 1Hrs/cycle		Non-operation
7	Vibration (With Carton)	1.5Grms, 10~200Hz Total time: 90 mins (30 mins/axis for X, Y, Z)		
8	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note 1 : T＝Ambient Temperature

Please follow Wahlee's main FPC design suggestion.
If you don't follow the Wahlee's main FPC design suggestion, then reliability items are not guaranteed.

F. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

H. Outline Dimension

Module Outline